A 1.62/2.7/5.4 Gbps Clock and Data Recovery Circuit for DisplayPort 1.2 with a single VCO

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Abstract—In this paper, a clock and data recovery (CDR) circuit that supports triple data rates of 1.62, 2.7, and 5.4 Gbps for DisplayPort 1.2 standard is described. The proposed CDR circuit covers three different operating frequencies with a single VCO switching the operating frequency by the 3-bit digital code. The prototype chip has been designed and verified using a 65 nm CMOS technology. The recovered-clock jitter with the data rates of 1.62/2.7/5.4 Gbps at $2^{31}-1$ PRBS is measured to $7/5.6/4.7$ ps$_{\text{rms}}$, respectively, while consuming 11 mW from a 1.2 V supply.

Index Terms—Clock and data recovery, voltage controlled oscillator, half-rate linear phase detector, DisplayPort1.2, display interface

I. INTRODUCTION

While the display technology is adapting high-performance flat-panel displays with advanced technologies, the need for a standard digital interface solution for improving performance has emerged. The DisplayPort, the display interface proposed by Video Electronics Standards Association (VESA), has been developed as the connectivity solutions such as PC, monitor, panel, projector and high definition content display, etc [1].

Clock and data recovery circuits (CDR) have found extensive applications in modern communication systems such as optical fiber, backplane routing, and interconnects between chips, etc. CDR circuit works at the receiver side of the serial interface to extract timing and data information from the transmitted data. The CDR also reduces jitter and skew in high speed serial links where a frequency offset may exist between the transmitter and the receiver [2].

Since the main link of DisplayPort 1.2 supports data rates of the 1.62/2.7/5.4 Gbps, the CDR at the receiver must be able to handle these data rates. So far, three different design approaches were used to generate multi-rate frequencies in CDR design. One is by a multi-path design in VCO [3]. The multi-path VCO requires more delay cells for more paths. The other approach is using a multi-load in VCO design [4]. The multi-load in VCO increases the capacitance of output node as more loads are used. It also requires more currents to drive each delay cell. The third approach used in reference [5] is the dual VCO’s to support three data rates. In this paper, a CDR circuit supporting three different frequencies with a single VCO is designed for DisplayPort 1.2 standard. The CDR designed with a multi-rate VCO adopts a multi-load with a reduced node capacitance by selecting a single load for a given operating frequency. This leads to a low power consumption CDR circuit. This paper is organized as follows. Section II describes the topology of the proposed CDR. Section III presents the building blocks of the circuit. In Section IV, the measurement results are given.

II. PROPOSED ARCHITECTURE

The architecture of the proposed CDR circuit is shown in Fig. 1. The proposed CDR is designed with a dual loop
structure with an external reference clock. The half-rate phase detecting operation relaxes the stringent speed requirement of the VCO.

The dual loop structure CDR using a single VCO incorporates frequency locked loop (FLL) and phase locked loop (PLL) for frequency and phase locking, respectively. The circuit first enables the FLL path for locking the VCO to the frequency of $N \times f_{ref}$. The lock detector monitors whether the output frequency of the VCO is close to the target frequency by comparing both the external reference clock and the output frequency of the VCO. When frequency error is near to a certain value, the FLL is shut down by the lock signal made by the lock detector. After the FLL path is locked, the PLL takes over to align the clock phase more precisely to the midpoint of the input data.

The mode selecting code is used for choosing the data rate among three different data rates. The ratio of divider in the FLL and the output frequency of the VCO are switched by the mode code bits. The ratio of the divider in the circuit is 6:1, 10:1, and 20:1, respectively, for the reference clock frequency 135 MHz, and the output frequency of VCO is 0.81/1.35/2.7 GHz at the data rate 1.62/2.7/5.4 Gbps with a half-rate PD, respectively.

III. CIRCUIT DESCRIPTION

1. Multi-rate VCO

In the proposed CDR architecture, the half-rate linear PD needs a half-rate clock signal from the VCO. It is also required for the VCO to provide three different output frequencies for supporting three input data rates for DisplayPort 1.2. The proposed multi-rate VCO generates three frequencies by selecting the designated load of the delay cell in the single VCO. The proposed VCO shown in Fig. 2 has a four-stage ring oscillator and generates different frequencies by the mode code bits. The delay cell of the proposed VCO is shown in Fig. 3. The different loads are selected based on the 3-bit mode code.

The switches connected to each load select a load and the PMOS transistor with control voltage ($V_c$) operates as a voltage controlled resistor. Since there is another PMOS controlled by the mode code, the VCO oscillates even if the control voltage is at $V_{DD}$. When the $V_c$ rises from 0V to $V_{DD}$, the resistance of PMOS increases and the output frequency of the VCO decreases. In contrast, when the $V_c$ drops to 0V, the output frequency of the VCO increases. In order to maintain a fixed output swing in wide frequency range, the current source transistor is biased in triode region.

$$T_{pd} = R_{load} \times C_{out}$$  \hspace{1cm} (1)

Eq. (1) tells that the load resistance and node capacitance decide a time delay($T_{pd}$) of each delay cell. When using the multi-load delay cell, the problem is that the node capacitance increases as the loads are added [4]. In this proposed VCO, the switch disconnects the non-selected loads from output node, which reduces
capacitances at the output node. This means that lower current is needed for the same data rate. And this also helps to determine the PMOS transistor size more easily for the target frequency compared to reference [4].

The required loop bandwidth of DisplayPort1.2 is defined as 5.4/10/10 MHz at a data rate 1.62/2.7/5.4 Gbps, respectively [1]. Setting the ratio of the VCO gain ($K_{vco}$) for 1.62 Gbps and 2.7/5.4 Gbps as approximately 1:1.8, respectively, the proposed CDR circuit employing a second-order loop filter satisfies the required loop bandwidth of each data rate. The simulation of the proposed VCO gain curve is given in Fig. 4. This shows the designed VCO satisfies three different target frequencies for all process corners (FF, TT and SS) under the given technology.

2. Divider

The phase-frequency detector (PFD) in the FLL path compares both the external reference clock and the divided clock from VCO. If a fixed rate reference clock is used, the divider in the FLL path must divide the output frequency of the VCO to three different rates since the proposed CDR is needed to support three data rates.

The divider circuit is shown in Fig. 5. This incorporates two divide-by-2 dividers, a divide-by-3 and a divide-by-5 divider. The switches in divide paths controlled by the mode code select only one divided clock signal for phase comparison. When the mode code is 100/010/001, the ratio of division is 6:1, 10:1 and 20:1, respectively. By sharing dividers, additional power consumption reduction is achieved. After frequency locked, the first /2 divider is turned off by the lock signal and then the operation of whole dividers is stopped for saving power consumption.

3. Phase Detector

The CDR circuits are using a binary (bang-bang or Alexander) PD or a linear (Hogge) PD. A linear PD has an advantage of presenting a straightforward design flow, since a typical linear PLL model fits the requirement well in the CDR design [6]. In addition, the CDR with a linear PD shows less ripple voltage on the control voltage to VCO than the bang-bang PD [7].

![Fig. 4. Simulated gain curve of the proposed VCO on three different process corners(FF, TT, SS).](image)

![Fig. 5. Divider circuit.](image)

![Fig. 6. Phase detector.](image)

In this design, a half-rate linear phase detector circuit is adopted. The block diagram of the half-rate linear PD which consists of four latches and two XOR gates is shown in Fig. 6. One of advantages of the half-rate PD is that the output frequency of VCO can be reduced by half because the half-rate PD uses both rising and falling edge of the clock. It relaxes the design effort of the VCO and decreases power consumption. In addition, the half-rate PD reduces one stage of DEMUXs for de-serialization because the output data is automatically de-serialized in the half-rate PD. The half-rate PD, however, could generate jitter if the clock duty cycle is distorted from 50%. Under this condition, the half-rate PD is not able to detect the exact mid-point of the input data as it uses both rising and falling edge of the clock. Therefore, the duty
corrector shown in Fig. 7 is used to achieve the duty cycle close to 50%. The circuit keeps the duty cycle close to 50% by stretching either “low” or “high” by forwarding the signals to each opposite lines.

4. Charge Pump

A charge pump circuit with NMOS current source is used as shown in Fig. 8. The structure sets the up current to be doubled than the down current because the pulse width of Y is a half of X. For avoiding the bias current mismatches, dummy transistors are placed around the current source transistor and the common-centroid methodology is used in the layout. Simulation shows the pumping currents are well matched within the locking voltage range as shown in Fig. 9.

5. Lock Detector

The lock detector circuit is shown in Fig. 10. The frequency lock detector keeps monitoring the difference between the reference clock and the multi-phases (CLK0, CLK90) of VCO. If the reference clock is placed between zero phase clock and 90 degree phase clock, the reset generator makes a reset signal to the counter. Since the 4-bit counter is used, the lock signal circuit generates the lock signal after 16 reset signals. That means the reference clock keeps the same position during continuous 16 reference clock period. The lock detector using multi-phases has proper margins for the different data rates and PVT variations [2].

IV. Measurement Results

The proposed CDR circuit has been fabricated using a 65 nm CMOS technology. The fabricated chip photo and the layout of the core block except the loop filter are shown in Fig. 11. The area of the core chip is 0.3 × 0.4 mm² including the loop filter and all pads include ESD protection circuits. The measurement was performed on a COB (Chip on board). The evaluation board is shown in Fig. 12. In the board, Ref_clk and Data_in signals are inputs, and R_clk (recovered clock) and R_data_even and R_data_odd (recovered data) are outputs. Since the recovered data are in a half-rate, two recovered data signals (Even, Odd) are taken out.

The reference clock and the PRBS (pseudo random binary sequence) pattern data are given by a function generator and a pulse pattern generator, respectively. A digital oscilloscope and a bit error detector are used to measure both data eye diagram and BER (bit error rate). The measurement setup is shown in Fig. 13. The measured eye diagrams of the recovered half-rate data
and the recovered clock jitter for the $2^{31}-1$ PRBS input data at 1.62/2.7/5.4 Gbps are shown in Fig. 14, respectively. The measured rms jitter of the recovered clock is 7/5.6/4.7 ps and the peak-to-peak jitter is 50/43.1/35.1 ps at 1.62/2.7/5.4 Gbps data rate, respectively.

Jitter tolerance testing has been conducted by following the compliance test specifications and Fig. 15 shows the measured results by applying a stressed signal of PRBS7 ($2^7$-1) data pattern. Stressed signal generator outputs PRBS7 pattern as defined in specification with Rj (random jitter), Sj (sinusoidal jitter), and ISI (intersymbol interference) jitter injected. The jitter tolerance test setup is shown in Fig. 13. The jitter tolerance tests the receiver ability to sustain a 10E-9 BER under the stressed signaling conditions. By the DisplayPort 1.2 compliance test specification (CTS) [8], the injecting jitter frequencies for jitter tolerance test are 2 MHz, 10 MHz, 20 MHz, and 100 MHz (2.7, 5.4 G only). During the test the total jitter components (ISI+Rj(RMS)+Sj) at different sinusoidal jitter (Sj) frequencies are generated by the stressed signal generator as specified by the CTS.

It can be seen that the proposed CDR satisfies the DisplayPort 1.2 jitter tolerance specifications for three different data rates. Due to the limitation of the jitter generation equipment at lower jitter frequency, the jitter amplitude at the frequency lower than 1MHz could not be generated [9]. Therefore the jitter tolerance was measured only over 1 MHz jitter frequency.

The proposed CDR circuit consumes 11 mW at 5.4 Gbps and shows a BER of less than $10^{-12}$ at the $2^{31}-1$
This work presents a CDR circuit which supports three different operating rates of 1.62/2.7/5.4 Gbps for DisplayPort 1.2 standard. The circuit used a half-rate PD and a single VCO covering three different data rates, which results in low power consumption. The VCO has the multi-load structure and reduces the node capacitance by selecting the only one load for the dedicated frequency. The prototype chip was fabricated using a 65 nm CMOS technology and the recovered-clock jitter with the data rates of 1.62/2.7/5.4 Gbps is measured to 7/5.6/4.7 ps, respectively, while consuming 11 mW from a 1.2 V supply.

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