Optimizing Effective Channel Length to Minimize Short Channel Effects in Sub-50 nm Single/Double Gate SOI MOSFETs

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Abstract—**In the present work a methodology to minimize short channel effects (SCEs) by modulating the effective channel length is proposed to design 25 nm single and double gate-source/drain underlap MOSFETs. The analysis is based on the evaluation of the ratio of effective channel length to natural/ characteristic length. Our results show that for this ratio to be greater than 2, steeper source/drain doping gradients along with wider source/drain roll-off widths will be required for both devices. In order to enhance short channel immunity, the ratio of source/drain roll-off width to lateral straggle should be greater than 2 for a wide range of source/drain doping gradients.**

Index Terms—**Short channel effect, source/drain profile optimization, double gate MOSFET, single gate MOSFET, silicon-on-insulator**

I. Introduction

Over the past few years Silicon-on-Insulator (SOI) based single and multiple-gate MOSFETs with fully depleted (FD) ultra-thin bodies (UTBs) have emerged as possible candidates for device scaling at the end of ITRS roadmap [1-2]. Amongst the many possible candidates, single and double gate SOI MOSFETs (Fig. 1(a) - (b)) have received considerable attention due to a relatively simple fabrication. However, as single and double gate MOSFETs are scaled down, short channel effects (SCEs) tend to degrade device performance [2]. Classically SCEs can be suppressed by designing devices such that the ratio of channel length to natural/characteristic length is greater than 1 [3].

Recently, the concept of "non-overlapped" gate-source/drain with low-doped channel was suggested [4-9] to facilitate the scaling of bulk-Si MOSFETs to nanoscale gate lengths. However, since short-channel effects (SCEs) in conventionally scaled bulk-Si MOSFETs are controlled predominantly via high channel doping [3], large gate-source/drain underlap are needed for acceptable SCE-control, and they result in suboptimal speed performance [4]. However, non-classical CMOS devices, e.g., fully depleted (FD) silicon-on-insulator (SOI) and double-gate (DG) MOSFETs, having ultra thin Si channels/bodies (UTBs) for SCE control, are being checked for scalability, and, because of technological limitations, the UTBs must be left undoped. The non-overlapped, or underlap, structure is therefore a possible design option for non-classical UTB MOSFETs. In gate-underlap architecture, source/drain doping profiles are designed such that the source/drain doping at the gate edge is well below the peak source/drain doping (~ 5×10^{20} cm^{-3}) i.e. the channel and extension regions adjacent to the gate are without any dopants [4].

In this paper, we use the expression of effective channel length for gate-source/drain underlap devices and natural/characteristic length scale for 25 nm single and double gate SOI MOSFETs to evaluate design

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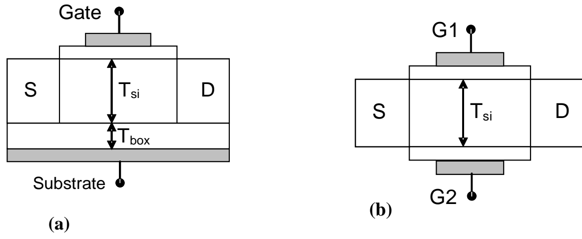

Fig. 1. (a) Schematic diagram of single gate (SG) SOI MOSFET. (b). Schematic diagram of double gate (DG) SOI MOSFET.

criterion to suppress SCEs. The optimal design guidelines are proposed for engineering the source/drain extension regions for 25 nm gate length single and double gate SOI MOSFETs. Results show that lateral source/drain doping gradient along with source/drain roll - off widths can be effectively used to suppress short channel effects in nanoscale devices. The present work provides valuable design insights in the performance of nanoscale DG SOI devices with optimal source/drain engineering and serves as a tool to optimise important device and technological parameters for 45 nm technology node.

II. Natural/Characteristic Length Scale

In order to analytically evaluate natural length scale of single and double gate SOI MOSFETs, we start from the 2D Poisson equation in silicon film in the weak inversion region, which is given as

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2}+\frac{\partial^2 \varphi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

where $\varphi(x,y)$ is the potential in the silicon film, q is the electron change, N_a is the doping in the silicon film (low doped) and ε_{si} is the permittivity of silicon film. Two-dimensional effects in SOI MOSFETs have been analyzed by various approaches [3, 10-16]. Young [10] proposed a parabolic function for potential distribution perpendicular to the channel, assuming that the electric field at the bottom of the silicon film was zero. Yan *et al* [3] extended the Young model and related the 2D potential distribution to the short channel effects and threshold voltage of the device. Suzuki *et al* [11-12] also used the parabolic approach to predict short channel effects in single and double gate MOSFETs. Banna *et al* [13] proposed a short channel model without assuming any perpendicular potential distribution in the silicon film. However, they neglected the 2D effects due to the drain bias at the bottom of the SOI layer. Further, a fitting parameter was used to obtain an agreement with the numerical data. In the present analysis, we use the superposition principle [14-16] to solve the 2D Poisson equation without any approximation for the potential distribution in the silicon film and derive an expression for the natural/characteristic length. The 2D potential ($\varphi(x, y)$) using the superposition principle is split into a long channel solution to the 1D Poisson equation ($\Psi(y)$) and a short channel solution to the 2D Laplace equation ($\chi(x, y)$) i.e. $\varphi(x, y) = \Psi(y) + \chi(x, y)$. The boundary conditions for the solution of (1) are given as

$$\left.\frac{d\varphi(x,y)}{dx}\right|_{y=0}=\frac{C_{fox}}{\varepsilon_{si}}\left(\varphi(x,y=0)-V'_{gs}\right) \quad (2a)$$

$$\left.\frac{d\varphi(x,y)}{dx}\right|_{y=Tsi}=\frac{-C_{box}}{\varepsilon_{si}}\left(\varphi(x,y=T_{si})-V'_{subs}\right) \quad (2b)$$

$$\varphi(x=0,y)=V_{bi} \quad (2c)$$

$$\varphi(x=L_{eff},y)=\varphi(x=0,y)+V_{ds} \quad (2d)$$

where $C_{fox} = \varepsilon_{ox}/T_{ox}$ and $C_{box} = \varepsilon_{ox}/T_{box}$ are the front and back gate oxide capacitances, respectively, T_{ox} is the front gate oxide thickness, T_{box} is the buried oxide thickness, C_{si} (= ε_{si}/T_{si}) is the silicon film capacitance, L_{eff} is the effective channel length (explained later), ε_{ox} and ε_{si} are the dielectric permittivities of oxide and silicon, respectively, $V'_{gs} = V_{gs} - V_{fb1}$ and $V'_{subs} = V_{subs} - V_{fb2}$ with V_{gs} and V_{subs} as the front and substrate gate voltages, respectively, and V_{fb1} and V_{fb2} as the front and back gate flatband voltages, respectively.

Solving (1) using (2), we obtain the potential distribution in the silicon film as

$$\varphi(x,y)=\sum_{n=1}^{\infty}\left(A_n\exp\left(k_n\left(x-L_{eff}\right)\right)+B_n\exp(-k_nx)\right)(\alpha_n)+\Psi(y) \quad (3)$$

where

$$\alpha_n=\left(\sin(k_ny)+\left(\frac{k_n\varepsilon_{si}}{C_{box}}\right)\cos(k_ny)\right)$$

$$\Psi(y)=\frac{qN_a}{\varepsilon_{si}}y^2+\frac{C_{fox}}{\varepsilon_{si}}\left(\gamma-V'_{gs}\right)y-\gamma$$

$$\gamma=\frac{V'_{gs}\left(\frac{C_{fox}}{C_{si}}+\frac{C_{fox}C_{box}}{C_{si}^2}+\frac{V'_{gs}}{V'_{subs}}\frac{C_{box}}{C_{si}}\right)-\left(\frac{qN_aT_{si}}{C_{si}}\right)\left(1+\frac{C_{box}}{2C_{si}}\right)}{\left(\frac{C_{fox}}{C_{si}}+\frac{C_{fox}C_{box}}{C_{si}^2}+\frac{C_{box}}{C_{si}}\right)}$$

$$A_n=\frac{1}{\exp(-2k_nL_{eff})-1}\left(\frac{\left(\int_0^{T_{si}}\chi(o,y)(\alpha_n)dy\right)\left((\exp(-k_nL_{eff})-1)\right)-\int_0^{T_{si}}V_{ds}(\alpha_n)dy}{\int_0^{T_{si}}\alpha_n^2dy}\right)$$

$$B_n=\frac{1}{\exp(-2k_nL_{eff})-1}\left(\frac{\left(\int_0^{T_{si}}\chi(o,y)(\alpha_n)dy\right)\left((\exp(-k_nL_{eff})-1)\right)-\left(\int_0^{T_{si}}V_{ds}(\alpha_n)dy\right)\left((\exp(-k_nL_{eff}))\right)}{\int_0^{T_{si}}\alpha_n^2dy}\right)$$

$$\chi(0,y)=V_{bi}-\Psi(y)$$

$$\chi(L_{eff},y)=V_{bi}+V_{ds}-\Psi(y) \tag{4}$$

and

$$\tan(k_nT_{si})=\frac{\left(C_{fox}+C_{box}\right)\left(k_n\varepsilon_{si}\right)}{k_n^2\varepsilon_{si}^2-C_{fox}C_{box}} \tag{5}$$

Equation (5) represents the eigenvalues equation which will be used to determine natural/characteristic length scale [17-19] for single gate SOI MOSFET. Using a similar approach, we obtain the eigenvalues equation for a double gate (T_{box} = T_{fox}, V_{gs} = V_{sub}) SOI MOSFET as

$$\tan(k_nT_{si})=\frac{\left(2C_{fox}\right)\left(k_n\varepsilon_{si}\right)}{k_n^2\varepsilon_{si}^2-C^2_{fox}} \tag{6}$$

The characteristic/natural length is calculated as $\lambda_n=n\pi/k_n$ [18] for both single and double gate MOSFETs. Please note that equation (5) is used to evaluate natural length scale for single gate SOI devices whereas equation (6) is applied for double gate MOSFETs. Since λ_n depends on T_{si} and T_{ox}, it provides a measure of short channel effects in a given structure and thus can be interpreted as the short channel immunity factor of a given structure [3]. The product L_{eff}/λ_1 must be greater than 2 to avoid SCEs in a given design [14-16]. Effective channel length (L_{eff}) is discussed in section 3.

III. Effective Channel Length in Gate-Source/Drain Underlap Devices

In the present work, we have modeled the effective channel length in gate-source/drain underlap devices (single and double gate MOSFETs) using the expression presented in [14] and is given as

$$L_{eff}=L_g+2\left(s-\sigma\sqrt{\ln\left(N_{SD}/\eta_{SD}\right)}\right) \tag{7}$$

where L_g is the gate length, s is the source/drain roll-off width (also called as the spacer width), σ is the technological parameter governing the source/drain profile roll-off $\left(\sigma=\sqrt{2sd/\ln(10)}\right)$ [14], d is the source/drain doping gradient (expressed in nm/decade) at the gate edge and η_{SD} is the source/drain doping level at which L_{eff} is extracted and is given as

$$\eta_{SD}=\eta_1\left(\ln\left(L_g/s\right)\right)+\eta_2 \tag{8}$$

where η_1 and η_2 are given as 2.25×10^{19} cm^{-3} and 1.5×10^{19} cm^{-3} [14] respectively. η_{SD} is a function of the spacer width to account for the fact that for larger spacer regions, the gate does not control the extension regions effectively. For s/L_g =0.25, η_{SD} evaluates to ~ 4.5×10^{19} cm^{-3} whereas for wider spacers (s/L_g =0.25) η_{SD} is 1.5×10^{19} cm^{-3} [14]. The depletion layer boundary at the source (or drain) edge depends on s and d. Therefore, the contribution of underlap region to L_{eff} can be taken as the distance from the depletion layer boundary (at source or drain end) to the gate edge. This has been approximated through the parameter η_{SD} in the expression of L_{eff}, i.e., the depletion region boundary at the source (or drain) end is evaluated in terms of an effective source/drain doping level (η_{SD}) [15]. Moreover, from (7) it can be seen that for large source/drain doping gradients (d) and smaller roll-off width (s), the second term $2\left(s-\sigma\sqrt{\ln\left(N_{SD}/\eta_{SD}\right)}\right)$ becomes negative, thus implying that L_{eff} is smaller than the physical gate length (L_g) whereas for larger spacers, L_{eff} > L_g. The later case of L_{eff} > L_g is referred as the gate-source/drain underlap design. Source/drain profile was modeled using the expression $N_{SD}(x)$ = $((N_{SD})_{peak})\exp(-x^2/\sigma^2)$, where $(N_{SD})_{peak}$ is the peak source/drain doping and d the

source/drain doping gradient evaluated at the gate edge as $d = 1/\left| dN_{SD}(x)/dx \right|$.

IV. RESULTS AND DISCUSSION

Fig. 2 shows the comparison between the eigenvalues determined by our approach and using the expression in [18]. Our results are in good agreement with those derived by Frank *et al.* [18] by solving the 2D Poisson's equation in the oxide and silicon regions. This shows that for the device parameters considered in the present work, solving the 2D Poisson's equation only in the silicon film itself is sufficient to provide a reasonable estimation of SCEs in DG MOSFETs. We have restricted our analysis to SiO_2 as the gate dielectric and therefore equation (6) is reasonable to estimate the natural/characteristic length in a given structure.

Fig. 3(a)-(b) show the variation of source/drain doping profile at two different doping gradients (3 and 5 nm/decade) and spacer widths (12.5 and 25 nm). A variation of source/drain roll-off widths (s) along with lateral source/drain doping gradient (d) results in the modulation of effective channel length (L_{eff}) in a nanoscale non-classical (gate underlap) single and double gate MOSFET. Wider roll-off widths (s) along with steeper doping gradient (lower d values) result in a longer effective channel length (L_{eff}) whereas a shorter spacer width along with gradual doping gradient (higher d values) yields shorter L_{eff}. It is important to note that the optimisation of s and d for short channel immunity must be considered along with T_{si}, T_{fox} and T_{box}, key structural parameters for single and double gate MOSFETs.

Fig. 4 shows the dependence of the ratio of effective channel length to gate length (L_{eff}/L_g) for L_g = 25 nm as a function of source/drain doping gradient (d) for various s values. The ratio L_{eff}/L_g higher than 1 indicate $L_{eff} > L_g$ whereas L_{eff}/L_g lower than 1 represent $L_{eff} < L_g$. It should be noted that for gate-source/drain underlap devices L_{eff} must be longer than L_g whereas $L_{eff} < L_g$ signify gate-source/drain overlap devices. The variation of source/drain roll-off width (s) along with lateral source/drain doping gradient (d) results in the modulation of L_{eff}. For devices designed with s > 25 nm, L_{eff}/L_g is greater than 1 for the entire range of d values. Ultra short channel devices should be designed with the ratio $L_{eff}/\lambda_1 > 2$ to suppress short channel effects [16]. Higher values of L_{eff}/λ_1 can be achieved (i) by increasing L_{eff} (for a constant L_g) and/or (ii) by decreasing λ_1. λ_1 depends on structural parameters such as T_{si} and T_{ox} whereas L_{eff} depends on s and d. As T_{ox} is governed by a technology, reducing T_{si} to limit short channel effects may not be a suitable option as it would

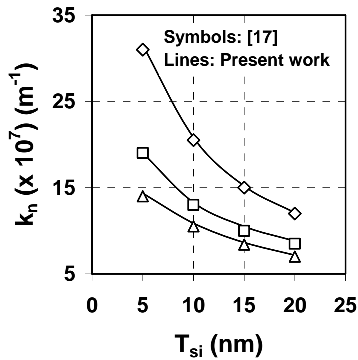

Fig. 2. Dependence of eigenvalues for DG MOSFET on silicon film thickness for various values of gate oxide thickness (◊ T_{ox} = 1 nm, □ T_{ox} = 3 nm and Δ T_{ox} = 5 nm).

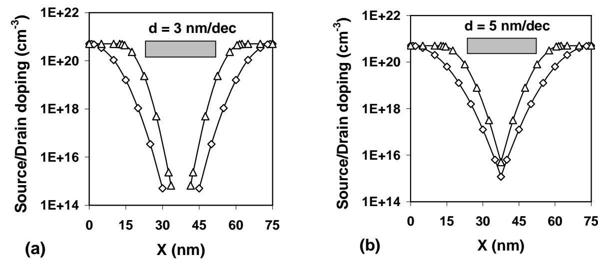

Fig. 3. (a) Dependence of source/drain doping profile along the channel direction at d = 3 nm/decade (◊ s = 25 nm and Δ s = 12.5 nm). (b) Dependence of source/drain doping profile along the channel direction at d = 5 nm/decade (◊ s = 25 nm and Δ s = 12.5 nm).

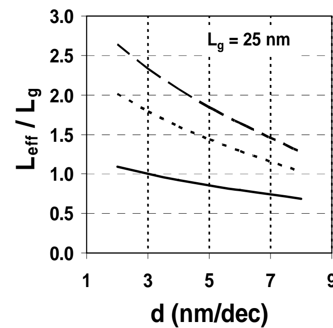

Fig. 4. Dependence of L_{eff}/L_g on d for various values of spacer widths (—— s = 12.5 nm, ... s = 25 nm and – – – s = 37.5 nm).

require a very high quality defect free film, which is still a technological challenge. Moreover, quantum effects, inversely proportional to film thickness, will be more significant. Therefore, the best compromise to minimize short channel effects in a given structure (for a fixed T_{ox} and T_{si}) is to modulate the effective channel length by varying the source/drain extension region parameters i.e. roll-off width and doping gradient.

Fig. 5(a)-(b) show the dependence of L_{eff}/λ as a function of silicon film thickness for various spacer widths and doping gradients in a single gate SOI MOSFET. The dashed rectangle in the figure represents the region where $L_{eff}/(\lambda_1)_{SG}$ is greater than 2 i.e. a useful design area to minimize short channel effects. Single gate SOI devices should be designed with T_{si} < 10 nm to achieve $L_{eff}/(\lambda_1)_{SG}$ > 2. A steeper d provides greater freedom in selecting s and T_{ox} values that result in $L_{eff}/(\lambda_1)_{SG}$ > 2. If d is fixed at 3 nm/dec, T_{si} can be varied from 5 to 10 nm for s = 37.5 nm whereas if d is increased to 5 nm/dec, the design flexibility in T_{si} is severely restricted to a single value of 5 nm. Devices designed with s = 12.5 nm will be unable to achieve $L_{eff}/(\lambda_1)_{SG}$ > 2 for any value of s, T_{ox} and d.

Fig. 6(a)-(b) shows the dependence of $L_{eff}/(\lambda_1)_{DG}$ on T_{si} for various values of s, d and T_{ox} for double gate devices. Double gate devices achieve lower values of λ_1 as compared to single gate devices because of better gate controllability. This results in higher values of

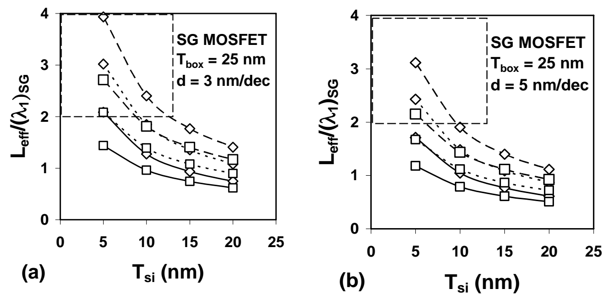

Fig. 5. (a) Variation of $L_{eff}/(\lambda_1)_{SG}$ with T_{si} at d = 3 nm/dec and T_{box} = 25 nm for single gate SOI MOSFET (◊ T_{ox} = 1 nm, □ T_{ox} = 3 nm, —— s = 12.5 nm, ... s = 25 nm and – – – s = 37.5 nm). The dashed rectangle represents the design space for which $L_{eff}/(\lambda_1)_{SG} \geq 2$. (b). Variation of $L_{eff}/(\lambda_1)_{SG}$ with T_{si} at d = 5 nm/dec and T_{box} = 25 nm for single gate SOI MOSFET (◊ T_{ox} = 1 nm, □ T_{ox} = 3 nm, —— s = 12.5 nm, ... s = 25 nm and – – – s = 37.5 nm). The dashed rectangle represents the design space for which $L_{eff}/(\lambda_1)_{SG} \geq 2$.

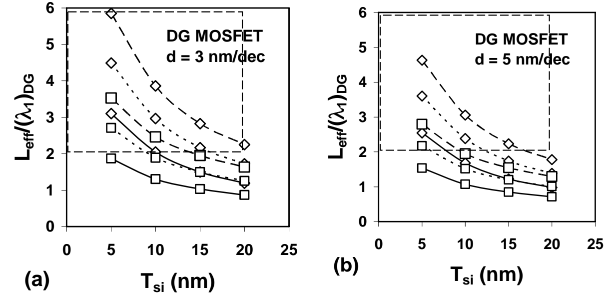

Fig. 6. (a) Variation of $L_{eff}/(\lambda_1)_{DG}$ with T_{si} at d = 3 nm/dec and T_{box} = 25 nm for double gate SOI MOSFET (◊ T_{ox} = 1 nm, □ T_{ox} = 3 nm, —— s = 12.5 nm, ... s = 25 nm and – – – s = 37.5 nm). The dashed rectangle represents the design space for which $L_{eff}/(\lambda_1)_{DG} \geq 2$. (b) Variation of $L_{eff}/(\lambda_1)_{DG}$ with T_{si} at d = 5 nm/dec and T_{box} = 25 nm for double gate SOI MOSFET (◊ T_{ox} = 1 nm, □ T_{ox} = 3 nm, —— s = 12.5 nm, ... s = 25 nm and – – – s = 37.5 nm). The dashed rectangle represents the design space for which $L_{eff}/(\lambda_1)_{DG} \geq 2$.

$L_{eff}/(\lambda_1)_{DG}$ as compared to single gate devices for the same set of device parameters (s, d, T_{si} and T_{ox}) and thus provide greater flexibility in selecting important device and technological parameters. DG devices are designed with d = 3 nm/dec, T_{ox} = 1 nm and s = 37.5 nm achieve $L_{eff}/(\lambda_1)_{DG}$ > 2 for almost the entire range of T_{si} (5 nm - 20 nm) where if T_{ox} is increased to 3 nm, T_{si} values must be limited to 15 nm to achieve $L_{eff}/(\lambda_1)_{DG}$ > 2 with d = 3 nm/dec. If d is increased to 5 nm/dec, T_{si} must be limited to 15 nm and 10 nm for T_{ox} = 1 nm and 3 nm respectively, for s = 37.5 nm in order to achieve $L_{eff}/(\lambda_1)_{DG}$ > 2. DG devices designed with s = 12.5 nm with T_{ox} = 3 nm will show severe short channel effects as $L_{eff}/(\lambda_1)_{DG}$ < 2 for the entire range of T_{si} and d. Devices designed with steeper doping gradients (d ~ 3 nm/dec) show flexibility in terms of thicker values T_{si} and T_{ox} to meet the criterion $L_{eff}/(\lambda_1)_{DG}$.

Although the expression of effective channel length was proposed by Kranti *et al.* [14-15], we provide further insights into the design of gate-underlap MOSFETs. Fossum *et al.* [4] qualitatively estimated the effective channel length (L_{eff}) in the subthreshold region (off-state) as L_g+2s. This qualitative estimation is suitable for general understanding but it neglects the fact that the depletion boundary edge towards the source and drain i.e. along the channel will not be located at the beginning of the underlap region rather at some distance away due to the non-abrupt nature of source/drain

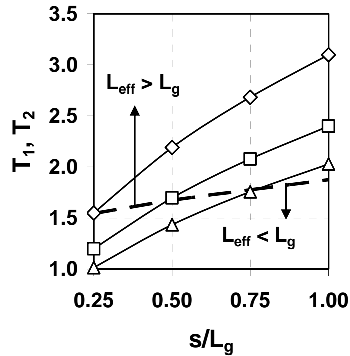

Fig. 7. Variation of T_1 (= s/σ, represented by symbols and solid lines) and T_2 (= $\sqrt{\ln(N_{SD}/\eta_{SD})}$, shown by dashed line) on s/L_g ratio for various values of doping gradients (d) (◊ d = 3 nm/dec, □ d = 5 nm/dec and Δ d = 7 nm/dec).

profile. The "true" contribution of each spacer region (i.e. towards the source and drain) can be written as

$$\frac{\Delta L}{2} = s\left(1 - (\sigma/s)\sqrt{\ln(N_{SD}/\eta_{SD})}\right) \quad (8)$$

From the above equation, it is clear that in order to achieve $L_{eff} > L_g$, the second term on the right hand side should be positive i.e. ΔL is positive. As shown in Fig. 7, a choice of underlap region parameters (s, d and σ), such that $s/\sigma < 1.5$ will yield $L_{eff} < L_g$ for doping gradients in the range of 3 - 7 nm/dec whereas the choice of $s/\sigma > 2$ results in $L_{eff} > L_g$ for the same range of doping gradients. Gate-underlap devices designed with $s/\sigma < 2.0$ perform worse than devices with abrupt SDE regions because a large d at lower σ causes dopant spill into the channel, leading to severe short channel effects. As the value of d depends on thermal budget and diffusivity, very small values (< 3 nm/dec) may be difficult to achieve (very small values of d require non-standard process [20-21] such as solid phase epitaxy or laser thermal annealing), as it may ultimately require control of individual atoms. Therefore, in order to design devices with higher s/σ values, it is more appropriate to increase the roll-off width in an optimal underlap design.

It should be noted that (i) devices designed with larger spacer widths ($s/L_g \geq 1$) and steeper doping gradients (d ~ 3 nm/dec) achieve L_{eff}/λ (for SG and DG devices) > 2, a key requirement for suppressing short channel effects and (ii) many different combinations of spacer and doping gradient yield $L_{eff}/\lambda > 2$. Devices with wider spacers lead to suppressed SCEs as $L_{eff}/(\lambda_1)_{SG}$ and $L_{eff}/(\lambda_1)_{DG} > 2$ but the longer L_{eff} will lower the on-current. Therefore, in an optimal design, the minimum value of spacer width (for a given doping gradient) that results in $L_{eff}/(\lambda_1)_{SG}$ or $L_{eff}/(\lambda_1)_{DG} > 2$ should be selected to minimize the off-current (reduce SCEs). The proposed analysis aids in selecting such possible spacer and gradient values, thus minimizing the design trade-off between acceptable SCEs and parasitic series resistance. Also, it has been demonstrated by 2D numerical simulations that optimally designed underlap devices can result in a minimal on-current reduction (15 - 25 %) with a substantial off-current reduction by nearly two orders of magnitude [14]. Underlap DG devices designed with $s/\sigma \sim 2.3$ have shown to be useful for achieving HP ITRS projections for on-current, off-current, intrinsic delay and on-off current ratio [22]. It is also worth mentioning that underlap devices with wider spacers ($s/L_g \geq 1$) are most useful for low voltage/power analog [23] and LOP/LSTP applications [22].

V. CONCLUSIONS

A comprehensive analysis of short channel effects in gate-source/drain underlap single and double gate SOI MOSFETs has been presented. Double gate devices exhibit higher design flexibility in selecting thicker values of silicon film thickness and gate oxide thickness in order to suppress short channel effects. 25 nm single gate devices must be designed with silicon film thickness limited to 10 nm with gate oxide thickness of 1 nm in order to satisfy the design criterion $L_{eff}/(\lambda_1)_{SG} >$ 2. In order to achieve $L_{eff} > L_g$ i.e. an effective underlap architecture instead of an overlap design, source/drain extension region should be designed such that $s/\sigma \geq 2$ for d lying between 3-7 nm/decade. Results presented in this work will be useful in design and optimization of nanoscale single and double gate SOI MOSFETs.

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