

# Editorial



It is a great honor and pleasure for me to serve as Guest Editor of this Special Issue of JSTS on the 2007 International SoC Design Conference (ISOCC2007). Among the total of 125 papers presented at the ISOCC2007, 8 outstanding papers were solicited for publication in this Special Issue.



The first paper authored by S. Heo and Y. Shin proposes a minimizing leakage of sequential circuits through flip-flop skewing and technology mapping to reduce designer's efforts and align well with traditional VLSI design process. The next paper by S. Chun et al. presents a new scan chain fault simulation method for scan chain diagnosis. The third paper written by C. Wu and J. Wu discusses a design of vector register architecture in DSP processor for efficient multimedia processing. The following paper by S. Lee et al. addresses a SSN-Reduced 5Gb/s parallel transmitter that is implemented with simplified logic circuits. The subject of the fifth paper authored by K. Kim et al. is phase-locked loop with leakage and power/ground noise compensation in 32nm technology.

A high throughput multiple transform architecture for H.264/AVC fidelity range extensions is reported in the sixth paper contributed by Y. Ma et al. The next paper by M. Hwang et al. deals with nanochannels for single DNA analysis using fabrication methods. The topic of the last paper suggested by T. Kim et al. in this Special Issue is a signal transient and crosstalk model of capacitively and inductively coupled VLSI interconnect lines.

I would like to express my deep gratitude to all the authors for having submitted high-quality papers to this Special Issue.

Kyu-Myung Choi  
Guest Editor  
CAE Team, System-LSI Division, Samsung ElectronicsKorea

Eui-young Chung  
Guest Editor  
Yousei University 134 Sinchon-Dong, Seodaemun-Gu, Seoul, Korea

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