

Compact Gate Capacitance Model with Polysilicon Depletion Effect for MOS Device

H. Abebe*, H. Morris, E.**, Cumberbatch***, and V. Tyree*

Abstract—The MOS gate capacitance model presented here is determined by directly solving the coupled Poisson equations on the poly and silicon sides, and includes the polysilicon (poly) gate depletion effect. Our compact gate capacitance model exhibits an excellent fit with measured data and parameter values extracted from data are physically acceptable. The data are collected from 0.5, 0.35, 0.25 and 0.18 μm CMOS technologies.

Index Terms—Device modeling, gate capacitance, MOSFETs, polysilicon depletion effect.

I. INTRODUCTION

The assumption in earlier MOS device modeling approaches is to treat the gate as a perfect conductor which would not deplete because the poly is heavily doped compared to the transistor channel. This assumption of a perfect conductor is no longer valid for current deep sub-micron processes. As the oxide thickness gets smaller, the silicon doping in the channel is increased to allow suitable channel control and these circumstances generate higher poly depletion at the gate, [1-4]. The performance degradations of the MOS device, reduced channel charge and gate capacitance result from an increase in channel doping and a decrease in the oxide thickness for a given poly doping [2-7].

The numerical solutions of (1) indicate that the poly depletion mainly affects the electrostatic potential at the poly/silicon-oxide interface rather than the surface potential at the silicon/silicon-oxide interface. A complete numerical simulation result of (1) is shown in [11]. Our work here focuses on developing a computationally efficient compact physical model for circuit simulation and other applications. The compact model presented here neglects the poly depletion effect on the surface potential at the silicon/silicon-oxide interface as a first order approximation.

II. MODEL EQUATIONS

Using the gradual channel approximation the coupled one-dimensional Poisson equations for the poly and silicon regions are written as

$$\frac{d^2V}{dX^2} = \frac{q}{\epsilon_{si}} \begin{cases} n - p - N_d & X \leq -T_{ox} \\ n - p + N_a & X \geq 0 \end{cases} \quad (1)$$

where $n = n_i e^{(V - \phi_n)/V_{th}}$ is electron density, $p = n_i e^{-(V - \phi_p)/V_{th}}$ is hole density, n_i intrinsic density, T_{ox} is the silicon-oxide thickness, $V(X)$ is the electrostatic potential; X is the perpendicular distance from the gate to silicon substrate N_d and N_a are the donor and acceptor doping densities respectively, q represents electron charge, ϵ_{si} semiconductor permittivity, ϕ quasi-Fermi potential, $V_{th} = k_b T / q$, k_b Boltzmann constant and T temperature. Both the poly and the silicon doping are considered to be uniform and separated by a thin oxide layer. The assumption here is that the doping density $N_d \gg N_a$ in the poly and $N_a \gg N_d$ in the silicon.

Manuscript received May 29, 2007; revised Aug. 10, 2007.

* University of Southern California Information Sciences Institute, MOSIS service, 4676 Admiralty Way, Marina del Rey, CA 90292, U.S.A

E-mail: abeb@mosis.org, tyree@ISI.edu

** San Jose State University, San Jose, CA 95192, U.S.A

E-mail: morris@math.sjsu.edu

*** Claremont Graduate University, Claremont, CA 91711, U.S.A

E-mail: ellis.cumberbatch@cgu.edu

In this work dimensional voltages and lengths are denoted by capital letters, and lower-case letters denote the same quantities non-dimensionalised. The voltage $V_{th} \ln \lambda$ is used as reference for voltages and potentials, the length value $L_d \sqrt{\ln \lambda / \lambda}$ is used as reference length, where $\lambda = N_a / n_i$ ranges from 10^5 to 10^8 , and $L_d = \sqrt{\epsilon_{si} V_{th} / q n_i}$ is the intrinsic Debye length. The gate oxide capacitance is scaled as $C_{ox} = c_{ox} \epsilon_{si} / L_d = \epsilon_{ox} / T_{ox}$. The boundary conditions consist of the continuity of electric potential V and electric displacement, $\epsilon dV/dX$, at the oxide interfaces $X=0, -T_{ox}$. Moreover the electric displacements at the two interfaces are equal. The electric potential and electric field are also considered to be zero in the bulk. The electrostatic potential V away from the interface at the edge of depleted poly gate is the applied gate voltage (V_g) minus the flat band voltage (V_{fb}). The flat band voltage represents the built-in potential or work function differences across the oxide interfaces, [8].

Using the scaling above, equation (1) becomes

$$\frac{d^2 v}{dx^2} = \begin{cases} \frac{1}{\beta} e^{(v-v_g^*) \ln \lambda} - \beta e^{-(v+2-v_g^*) \ln \lambda} - 1/\beta & x \leq -t_{ox} \\ e^{(v-2) \ln \lambda} - e^{-v \ln \lambda} + 1 & x \geq 0 \end{cases} \quad (2)$$

where $\beta = N_a / N_d$, v_g^* is the gate voltage minus the flat band voltage, and at thermal equilibrium the electron and hole quasi-Fermi potentials are equal. The quasi-Fermi potential is taken to be unity in the silicon substrate and it is $1 + v_g^* - v_{bi}$ at the poly gate where $v_{bi} = 2 - (\ln(\beta)) / \ln \lambda$ is the built-in potential. Integration of (2) and application of the boundary conditions at the bulk and poly gate, give

$$\left. \frac{dv}{dx} \right|_{x=-t_{ox}} = \sqrt{\frac{2}{\beta \ln \lambda} (e^{(v_i-v_g^*) \ln \lambda} - 1) + \frac{2\beta}{\ln \lambda} (e^{-(v_i+2-v_g^*) \ln \lambda} - \frac{1}{\lambda^2}) - \frac{2}{\beta} (v_i - v_g^*)} \quad (3a)$$

$$\left. \frac{dv}{dx} \right|_{x=0} = \sqrt{\frac{2}{\ln \lambda} (e^{(v_i-2) \ln \lambda} + e^{-v_i \ln \lambda} - \frac{1}{\lambda^2} - 1) + 2v_i} \quad (3b)$$

Boundary conditions at the oxide interfaces yield

$$\left. \frac{dv}{dx} \right|_{x=-t_{ox}} = \left. \frac{dv}{dx} \right|_{x=0} = c_{ox} \sqrt{\frac{\ln \lambda}{\lambda}} (v_s - v_t) \quad (4)$$

where $v_s = v(0)$ and $v_t = v(-t_{ox})$

Equations (3) and (4) give

$$q_g^2 = \frac{2}{\beta \ln \lambda} (e^{(v_i-v_g^*) \ln \lambda} - 1) + \frac{2\beta}{\ln \lambda} (e^{-(v_i+2-v_g^*) \ln \lambda} - \frac{1}{\lambda^2}) - \frac{2}{\beta} (v_i - v_g^*) \quad (5)$$

where $q_g^2 = \frac{2}{\ln \lambda} (e^{(v_i-2) \ln \lambda} + e^{-v_i \ln \lambda} - \frac{1}{\lambda^2} - 1) + 2v_i$ is known by neglecting the poly depletion effect on v_s as stated in the introduction. There are several methods to solve v_s without the poly depletion effect [9, 10]. A solution for v_s can be achieved in replacing v_t by v_g^* in (4) and solving (3b).

The gate capacitance is defined as

$$C = \frac{dQ_g}{dV_{gs}} \quad (6)$$

where $Q_g = A \cdot (v_s - v_t) V_{th} \ln \lambda \cdot c_{ox} \epsilon_{si} / L_d$ and A is the capacitance area. Both v_s and v_t depend on the gate voltage and a closed form of the capacitance can be determined from the derivatives with respect to the gate voltage.

The solution for v_t is determined from the transcendental equation (5) using Newton's method, and convergence is achieved with a maximum of two iterations

$$v_t = v_1 - \frac{g(v_1)}{g'(v_1)} \quad (7)$$

Where

$$v_1 = v_0 - \frac{g(v_0)}{g'(v_0)}, \quad v_0 = v_g^* - \frac{q_g^2 \beta}{2},$$

$$g(v_i) = q_g^2 - \frac{2}{\beta \ln \lambda} (e^{(v_i-v_g^*) \ln \lambda} - 1) - \frac{2\beta}{\ln \lambda} (e^{-(v_i+2-v_g^*) \ln \lambda} - \frac{1}{\lambda^2}) + \frac{2}{\beta} (v_i - v_g^*),$$

$$g'(v_i) = \frac{dq_g^2}{dv_s} \frac{dv_s}{dv_i} - \frac{2}{\beta} e^{(v_i - v_g^*) \ln \lambda} + 2\beta e^{-(v_i + 2 - v_g^*) \ln \lambda} + \frac{2}{\beta},$$

$$\frac{dq_g^2}{dv_s} = 2e^{(v_s - v_g^*) \ln \lambda} - 2 \ln \lambda e^{-v_s \ln \lambda} + 2,$$

$$\frac{dv_s}{dv_i} = 1 + \frac{\frac{\sqrt{\lambda}}{c_{ox}} \left(\frac{1}{\beta} e^{(v_i - v_g^*) \ln \lambda} - \beta e^{-(v_i + 2 - v_g^*) \ln \lambda} - \frac{1}{\beta} \right)}{\sqrt{\frac{2}{\beta} (e^{(v_i - v_g^*) \ln \lambda} - 1) + 2\beta (e^{-(v_i + 2 - v_g^*) \ln \lambda} - \frac{1}{\lambda^2}) - \frac{2 \ln \lambda}{\beta} (v_i - v_g^*)}}$$

Equation (7) is valid for all device operational regions: accumulation, depletion and inversion. In accumulation, holes are at the device channel surface to provide a net positive charge, at depletion the bulk charge dominates, and electrons provide a net negative charge in the inversion case.

III. RESULTS

The gate capacitance model in (6) gives accurate results for the poly depletion effect (see Table. 1 and comparison with measured data in Figure 1).

Table 1. Model parameters extracted from different technology data.

Tech (μm)	Na (m-3) × 10 ²³	Nd (m-3) × 10 ²⁶	Tox (nm)	Vfb (V)
0.18	1.41316	1.40342	3.8870	-0.94
0.25	1.29405	14.0368	5.6094	-0.97
0.35	0.521136	8.4875	7.6198	-0.76
0.5	0.068964	11.2137	14.050	-0.46

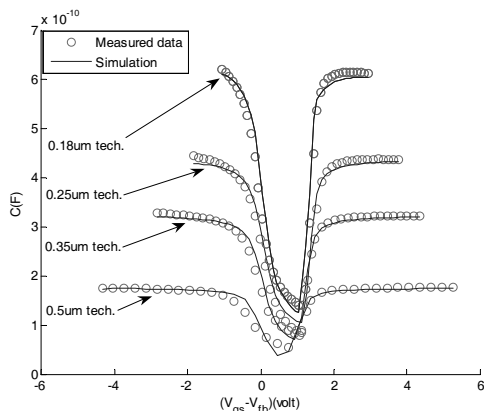


Fig. 1. MOS gate capacitance versus relative gate voltage.

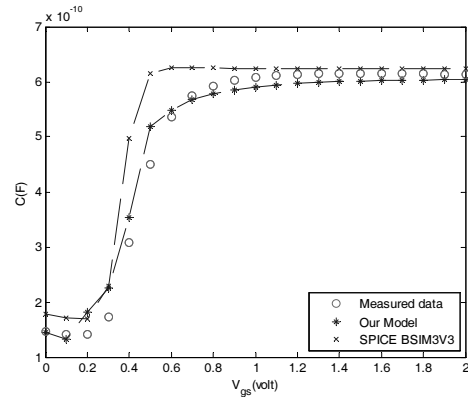


Fig. 2. MOS gate capacitance versus applied gate voltage comparison of the 0.18um tech.

In Figure 2 we compared our model with the industry standard SPICE BSIM3v3 model extracted from the same wafer lot of the 0.18um technology C-V measured data and our model simulation gives improved results. This new information may be used to improve circuit simulations in advanced VLSI since the gate depletion effect is significant in the current MOS devices.

ACKNOWLEDGMENTS

This work was supported by MOSIS service. The authors would like to thank Cesar Pina for funding the work.

REFERENCES

- [1] N. Arora and C. Huang, "Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance," *IEEE Transactions on Electron Devices*, Vol. 42, No. 5, May (1995).
- [2] R. Rios, N. D. Arora and C. L. Huang, "An Analytic polysilicon depletion effect model for MOSFET's," *IEEE Electron Device Letters*, Vol. 15, No. 4, April (1994).
- [3] G. Gildenblat, T. L. Chen and P. Bendix, "Analytical application for perturbation of MOSFET surface potential by polysilicon depletion layer," *IEE Electronic Letters*, Vol.. 35, No. 22, 28th October (1999).

- [4] C.-H. Choi et al., "Gate length dependent polysilicon depletion effects," *IEEE Electron Device Letters*, Vol. 23, No. 4, April (2002).
- [5] S. Lo, D. Buchanan, and Y. Taur, "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides." *IBM J. Res. Develop.* Vol. 43, No. 3, May (1999).
- [6] A. Gupta et al., "Accurate determination of ultrathin gate oxide thickness and effective polysilicon doping of CMOS devices," *IEEE Electron Device Letters*, Vol. 18, No. 12, December (1997).
- [7] F. Gamiz et al., "Effect of polysilicon depletion charge on electron mobility in ultrathin oxide MOSFETs," *Semiconductor Science and Technology*, Vol. 18, No. 11, November (2003).
- [8] R. F. Pierret, *Field Effect Devices*, Addison-Wesley, second edition, Vol. IV, (1990).
- [9] T. L. Chen and G. Gildenblat, "Analytical approximation for the MOSFET surface potential," *Solid State Electronics*, 45, pp.335-339, (2001).
- [10] A. Ortiz-Conde, F. J. Garcia Sanchez, M. Guzman, "Exact Analytical Solution of Channel Surface Potential as an Explicit Function of Gate Voltage in Undoped-body MOSFETs Using the Lambert W function and a Threshold Voltage Definition," *Solid-State Electronics* 47 pp. 2067-2074 (2003).
- [11] H. Abebe, E. Cumberbatch, H. Morris and V. Tyree, "Numerical and analytical results of the polysilicon gate depletion effect on MOS gate capacitance," *IEEE UGIM Proceedings*, pp. 111-115, June 25-28, (2006), San Jose, CA.



Henok Abebe received a joint Ph.D. in Engineering and Industrial Applied Mathematics in 2002 and M.S in Mathematics in 1998 both from Claremont Graduate University, California. He received M.S in

physics with honors from California State University

Los Angeles in 1996 and B.S in physics from Addis Ababa University in 1987. He is a member of IEEE and has been publishing several research papers in international journals and conference proceedings. His research interests are in quantum mechanics, semiconductor device modeling and SPICE circuit simulation. Since 2000 he has been employed as a device modeling VLSI research engineer by the University of Southern California, Viterbi School of Engineering, Information Sciences Institute, MOSIS Service. Dr. Abebe is also working as adjunct faculty, teaching applied modern physics course, at California State University Los Angeles Department of Physics and Astronomy for several years.



Hedley Morris was born in London England, in 1947. He received both his BS degree in Mathematics in 1968 and his PhD in Theoretical Physics in 1971 from London University and his Sc.D. in Applied Mathematics from Trinity College Dublin in 1986. He is presently a Professor of Mathematics at Claremont Graduate University in California. Professor Morris is the author of a textbook on nonlinear waves and the editor of several other books. He is a member of IEEE and has published more than 70 research papers in international journals and conference proceedings. His present research interests include Semiconductor modeling, Image Processing and Financial Engineering.



Ellis Cumberbatch gained a BS in 1955 in Mathematics, and a PhD in Applied Mathematics in 1958, at the University of Manchester. He has taught in the Mathematics Departments of Leeds University, Purdue University, and Claremont Graduate University. His research interests are in mathematical modeling and in obtaining solutions to problems in fluid mechanics and in current flow in semi-conductor devices.



Vance Tyree serves as Research and Development Manager in The MOSIS Service with a wide range of responsibilities including various research tasks. He manages the wafer level characterization of parametric and reliability of wafers received from suppliers of fabricated CMOS and GaAs wafers. Parametric characterizations include measurement of parasitic components, device modeling, and special devices such as CCD image arrays and other optical sensors. Information from these characterizations is essential to the success of designs implemented by MOSIS customers. Research activities include the development of wafer level reliability and quality assurance procedures, and CMOS semiconductor device modeling. The CMOS device modeling work is aimed at improving the accuracy of CMOS SPICE circuit simulations with deep-submicrometer feature size transistors. The research investigating physical wear-out models is intended for use in the implementation of reliability simulation of new IC designs. In addition, he is responsible for the technical interaction between MOSIS and the fabrication contractors in areas of new technology interfaces. Mr. Tyree received the MSEE degree from the University of California, Berkeley.