

A Fully Integrated 5-GHz CMOS Power Amplifier for IEEE 802.11a WLAN Applications

Sang-Hyun Baek, Changkun Park, and Songcheol Hong

Abstract—A fully integrated 5-GHz CMOS power amplifier for IEEE 802.11a WLAN applications is implemented using 0.18- μm CMOS technology. An on-chip transmission-line transformer is used for output matching network and voltage combining. Input balun, inter-stage matching components, output transmission line transformer and RF chokes are fully integrated in the designed amplifier so that no external components are required. The power amplifier occupies a total area of $1.7\text{mm} \times 1.2\text{mm}$. At a 3.3-V supply voltage, the amplifier exhibits a 22.6-dBm output 1-dB compression point, 23.8-dBm saturated output power, 25-dB power gain. The measured power added efficiency (PAE) is 20.1% at max. peak, 18.8% at P1dB. When 54 Mbps/64 QAM OFDM signal is applied, the PA delivers 12dBm of average power at the EVM of -25dB.

Index Terms—CMOS power amplifier (PA), WLAN, transmission-line transformer (TLT), on-chip

I. INTRODUCTION

The growing demands for high data rate communication in WLAN has driven the market toward the 5GHz IEEE 802.11a and 802.11n [1]. These standards provide data rates up to 54 Mb/s using a 20MHz channel bandwidth in the 5GHz unlicensed national information infrastructure (UNII) band, which indicated different power values for the different sub-bands as shown in Fig. 1. These standards are based on orthogonal frequency

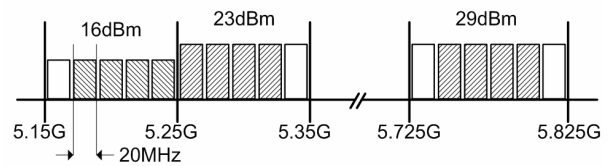


Fig. 1. Channel allocation and transmit powers of the IEEE 802.11a standard.

division multiplexing (OFDM) modulation consisting of 52 subcarriers, each subcarrier being either BPSK, QPSK, 16QAM, or 64QAM modulated.

OFDM systems require a very high peak-to-average ratio for the modulated signal to satisfy IEEE 802.11a linearity requirement. Therefore, the required maximum output power of the power amplifier should be much higher than the required average power of the PA. That is, the PA operates at backed off power.

In this paper, we present a fully integrated 5GHz CMOS power amplifier for IEEE 802.11a WLAN application that fulfills the backed-off requirements of 802.11a standard. The PA includes all elements on chip such as input balun, inter-stage matching network, output half-turn transformer (HTT).

II. POWER AMPLIFIER DESIGN

The PA is designed to operate over the range of 5.15GHz to 5.35GHz, which include the two bands for IEEE 802.11a standard using indoor application. Fig. 2 shows the schematic of the 5-GHz CMOS power amplifier designed for IEEE 802.11a WLAN applications. Using cascode configuration, we can have several benefits [2]. Due to good input/output isolation, stability can be improved. In addition, using 0.35 μm thick-oxide transistor as common-gate transistor increases the breakdown voltage and the operation

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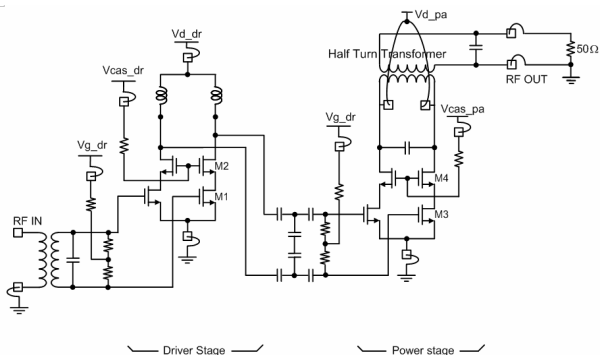


Fig. 2. Schematic of the two-stage differential CMOS power amplifier including input balun and half-turn transformer

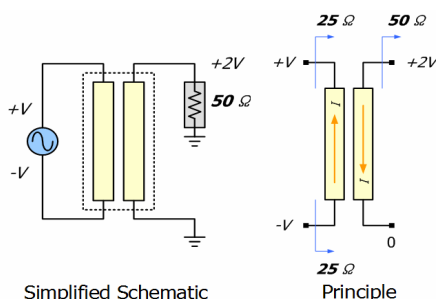


Fig. 3. Simplified schematic and operating principle of transmission-line transformer

voltage. Differential topology is used to minimize the effect of bond-wire inductors. This topology creates an ac virtual ground at the source node of common-source transistor and V_{dd} supply node. Class-AB biasing is chosen for this PA. Driver stage is biased at near class-B and power stage is biased at class-AB. This helps to increase 1-dB compression point (P_{1dB}) by combining gain-expansion and gain-compression.

Inductor components are eliminated in the inter-stage matching network for efficient layout and good stability. The output matching network is realized by a magnetically coupled half-turn transformer (HTT). Fig. 3 shows the simplified schematics and operating principle. This CMOS process used for the circuit provides 2-um thick Al metal layer. Due to thick metal, the loss of output transformer can be minimized. To predict the characteristics and performance of the output transformer, quasi-3D electro-magnetic (EM) simulation was performed using Ansoft Designer. From the simulation, the efficiency of the half-turn transformer can be achieved over 75%. With an additional shunt MIM capacitor, which has a higher Q than the slab inductor of HTT, the output matching network is fully integrated.

III. EXPERIMENTAL RESULTS

This circuit was implemented using TSMC 0.18um 1P6M CMOS process. A printed circuit board (PCB) for testing the power amplifier was also fabricated using TLX-9. The die photograph of the fabricated power amplifier is shown in Fig. 4. The chip size is 1.2mm \times 1.7mm. This circuit was tested at a 3.3V about both driver and power stage. The measured output power, power gain, PAE and drain efficiency are shown in Fig. 5. The frequency of the input signal is 5.25GHz, which is the center frequency in the range of 5.15GHz to 5.35GHz. With a supply voltage of 3.3V, the power amplifier consumes quiescent current of 260mA and provides power gain of 25dB and 1-dB compression point (P_{1dB}) of 22.6dBm. By setting the gate bias of the driver stage lower than that of power stage, some gain expansion occurs, which effectively increases P_{1dB} and improves the linearity characteristic of power amplifier. PAE of 18.8% is achieved at the P_{1dB} and maximum PAE is 20.1% at saturated output power of 23.8dBm. The measured data include the gain and power loss caused by the on-chip balun and bonding-wires. Fig. 6 shows measured output power and efficiency versus frequency of designed power amplifier. Over 200MHz band from 5.15GHz to 5.35GHz, flat output power and efficiency can be achieved. This is caused by broadband characteristic of half-turn transformer using as output matching. The Error Vector Magnitude (EVM) behaviour is shown as Fig. 7. It shows that the maximum average output power for a 54Mbps/64QAM signal is about 12dBm.

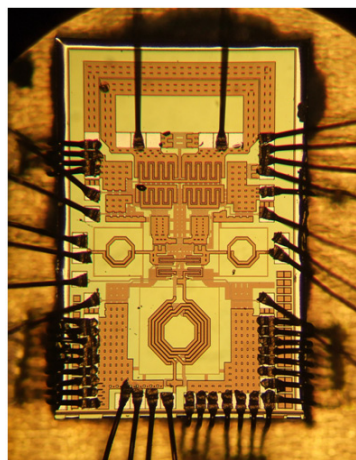


Fig. 4. Photograph of the fabricated power amplifier

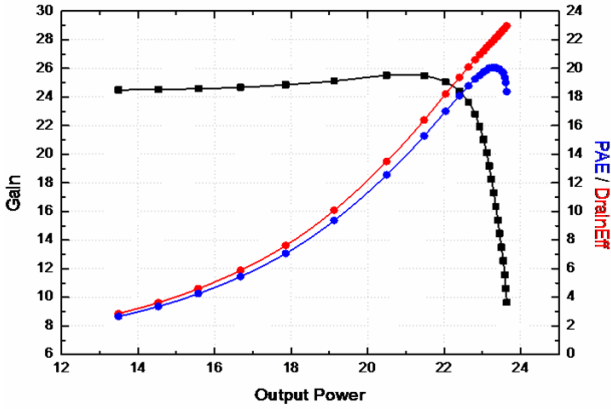


Fig. 5. Output power, gain, and PAE of the designed power amplifier when measured at 5.25GHz.

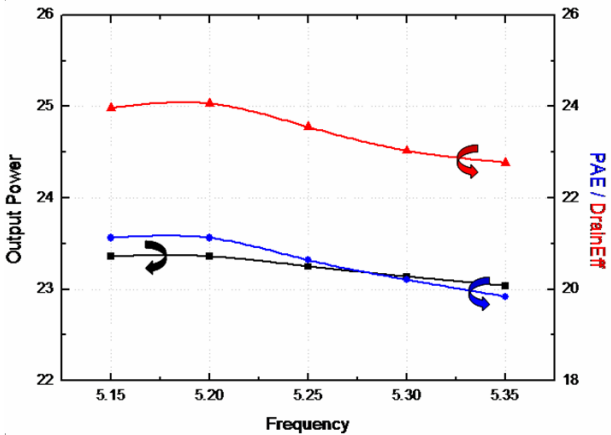


Fig. 6. Measured output power, PAE and drain efficiency of designed power amplifier over 5.15~5.35GHz freq. band

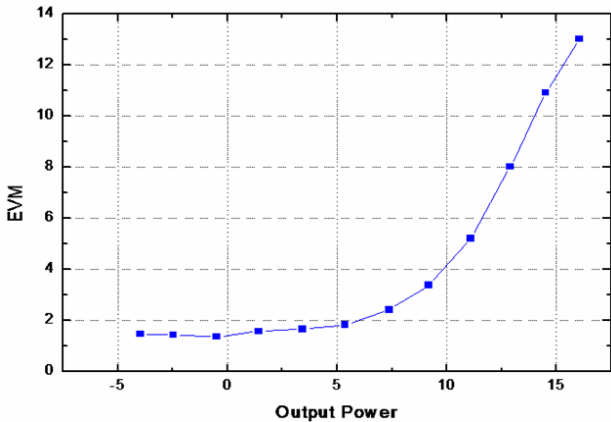


Fig. 7. Measured Error Vector Magnitude (EVM) vs. Average output power when 54Mbps/64QAM signal is applied.

IV. CONCLUSION

In this paper, a fully integrated 5GHz CMOS power amplifier for IEEE 802.11a applications has been demonstrated using 0.18μm CMOS technology. To

combine output power, transmission line transformer (TLT) is used. The maximum power is 23.8dBm and power added efficiencies are 18.8% at P1dB and 20.1% at P_{sat}, respectively. When 54 Mbps/64 QAM OFDM signal is applied, the PA delivers 12dBm of average power at the EVM of -25dB.

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