Threshold Voltage Modeling of Double-Gate MOSFETs by Considering Barrier Lowering

Byung-Kil Choi, Ki-Heung Park, Kyoung-Rok Han, Young Min Kim, and Jong-Ho Lee

***Abstract*—Threshold voltage (V_{th}) modeling of double-gate (DG) MOSFETs was performed, for the first time, by considering barrier lowering in the short channel devices. As the gate length of DG MOSFETs scales down, the overlapped charge-sharing length (x_h) in the channel which is related to the barrier lowering becomes very important. A fitting parameter δ_w was introduced semi-empirically with the fin body width and body doping concentration for higher accuracy. The V_{th} model predicted well the V_{th} behavior with fin body thickness, body doping concentration, and gate length. Our compact model makes an accurate V_{th} prediction of DG devices with the gate length up to 20-nm.**

***Index Terms*—Barrier lowering, Bulk FinFET, double-gate, modeling, threshold voltage**

I. INTRODUCTION

According to the projection of the 2007 International Technology Roadmap for Semiconductors (ITRS), the physical gate length of MOSFET for a microprocessor unit (MPU) can be scaled down to 18 nm in 2010 [1]. The scaling-down of devices is strongly required to achieve high integration density and performance.

Recently, bulk FinFETs have been considering very promising candidate for next generation memory cell transistors to be applicable to dynamic random access memory (DRAM) and flash memory [2]. As the gate length of bulk FinFETs [3]-[5] scales down, barrier lowering occurs in spite of low drain bias (V_{DS} =0.05 V) because the depleted charge-sharing length (x_h) [6] by sorce and drain in short channel is overlaped. To apply the devices to integrated circuits, it is strongly required to model threshold voltage (V_{th}) considering the barrier lowering in short channel. However, the V_{th} model has not been developed since the x_h modeling in short channel devices is very complicated with device geometry and doping concentration. For V_{th} modeling of the devices, double-gate (DG) nature is key point and needs to be understood well.

In this paper, we propose V_{th} model of DG MOSFETs [7], [8] based on the correction of x_h considering barrier lowering, and verify the V_{th} model by comparing with device simulation [9] in terms of gate length (L_g), fin width (W_{fin}) and body doping (N_b). Threshold voltages were extracted by using $g_{m,max}$ for a given V_{DS} of 0.05 V in this paper.

II. DEVICE STRUCTURE

Fig. 1 shows 3-D schematic view of the bulk FinFET. The H_g and W_{fin} represent gate height and fin width, respectively. The x_{jSDE} stands for junction depth of

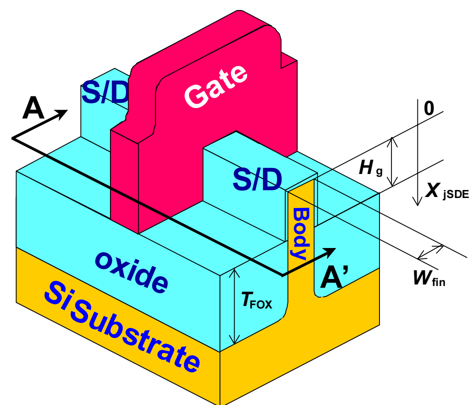

Fig. 1. 3-D schematic view of bulk FinFET. The H_g and W_{fin} represent fin height and width, respectively.

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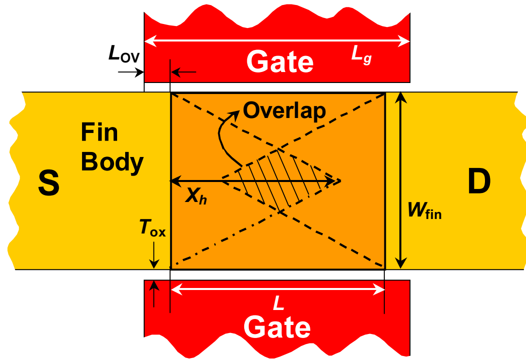

Fig. 2. 2-D cross-sectional view of the bulk FinFET along A-A' in Fig. 1. The T_{ox} and x_h represent gate oxide thickness and charge-sharing length, respectively.

source/drain extensions (SDE). The SDE concentration is 7×10^{19} cm^{-3} and has the profile of about dec/5 nm. Gate oxide thickness (T_{ox}) is fixed at 1.5 nm. T_{FOX} represents field oxide thickness for device isolation.

Fig. 2 shows 2-D schematic view of the DG MOSFET. Channel doping is uniform and a variable. n$^+$ poly gate was applied.

III. V$_{TH}$ MODEL AND VERIFICATION

Fig. 3 shows δ_w versus W_{fin} as a parameter of the body doping. Here, the δ_w [10] is a fitting parameter representing a difference between $V_{th,simulation}$ and $V_{th,model}$, and introduced to take into account the V_{th} change with the W_{fin}. A fitting parameter δ_w (empirical) is given by a kind of empirical equation based on various data. In Fig. 3, the empirical model (open symbols) shows a good agreement with the fitted data (solid symbols), and is given by

$$\delta_w = \left(-0.04461 - 0.00354\cdot\frac{N_b}{10^{18}} + 0.22176\times0.2564^{\frac{N_b}{10^{18}}}\right) + \left(0.00322 + 0.00008\cdot\frac{N_b}{10^{18}} - 3.50807\times0.0171^{\frac{N_b}{10^{18}}}\right)W_{fin} + \left(-0.00006 + 0.000006\cdot\frac{N_b}{10^{18}} + 0.00733\times0.0618^{\frac{N_b}{10^{18}}}\right)W_{fin}^2 . \quad (1)$$

In Fig. 2, as the L_g of the device scales down, the x_hs from the source and the drain are overlapped each other. The overlap of x_h means barrier lowering, and affects V_{th} behavior. Therefore, the V_{th} model of DG MOSFETs must be modified by taking into account barrier lowering

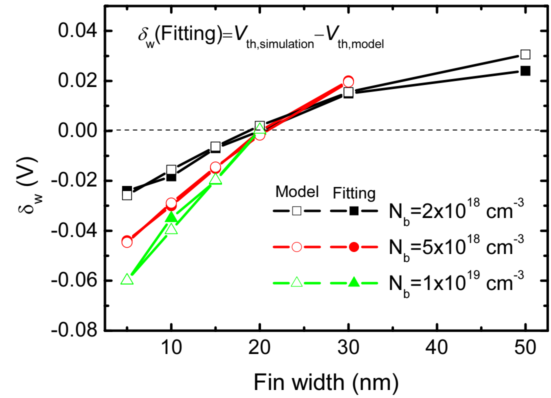

Fig. 3. δ_w versus fin width as a parameter of the body doping. The δ_w is obtained by subtracting the modeled V_{th} from the simulated V_{th}.

in x_h of short channel DG devices. To see an internal physics for the 20 nm device, we prepared Fig. 4 which shows the conduction band energy diagrams cut along the channel width direction at a point showing peak conduction band energy over the channel length at given V_{DS}=0.05 V and $V_{GS}=V_{th}$ condition. It is normal that the conduction band minimum is found at the channel surface in a device without barrier lowering. However, the 20 nm DG devices show the minimum point of the conduction band at the center of the body due to the barrier lowering. In Fig 5, we observe the conduction band energy starts to decrease when L_g decreases from 50 nm to 40 nm for given N_b of 2×10^{18} cm^{-3} and W_{fin} of 15 nm. This change corresponds exactly to the x_h overlap represented by dotted line in Fig. 9. The devices in both Figs. 5 and 9 have the same device geometry and body doping. Since the x_h' ($=x_h-\Delta x_h$) which is charge-sharing length considering barrier lowering is function of N_b, W_{fin}, and L_g, it is very difficult (or complicated) to derive an equation of x_h' based on physics. We performed device simulation extensively by changing 3 parameters mentioned above. Then we obtained a sort of empirical equation at a fixed N_b to explain x_h' for given W_{fin} and L_g by fitting the equation to the (x_h')s extracted from simulated data. As an example, an empirical x_h' for an N_b of 2×10^{18} cm^{-3} and L_g of 20 nm to 40 nm is given by

$$x_h' = (8.31586 + 0.52656\cdot L_g - 0.01177\cdot L_g^2) - (0.0401 + 0.00258\cdot L_g - 0.00021\cdot L_g^2)\cdot W_{fin} - (69.14274 - 4.86237\cdot L_g + 0.0389\cdot L_g^2) \times(1.23917 - 0.02648\cdot L_g + 0.0004\cdot L_g^2)^{W_{fin}} . \quad (2)$$

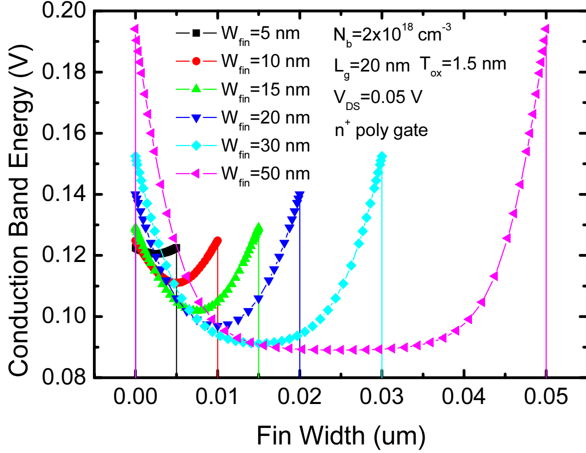

Fig. 4. Conduction band energy versus fin width as a parameter of W_{fin}. This figure shows conduction band energy diagrams cut along the channel width direction at a point showing peak conduction band energy over the channel length at V_{DS}=0.05 V and V_{GS}=V_{th} condition.

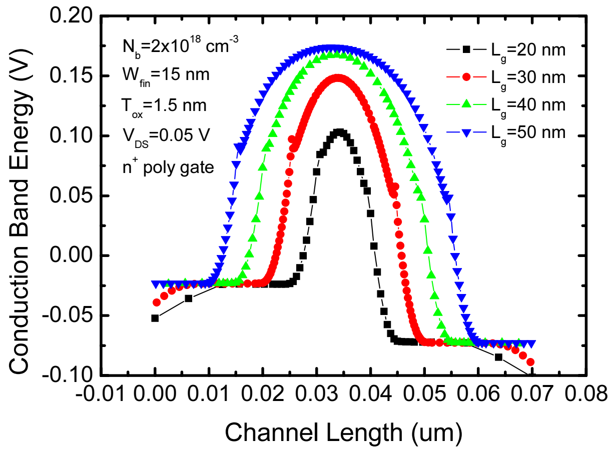

Fig. 5. Conduction band energy versus channel length as a parameter of L_{g}. This figure shows conduction band energy diagrams cut along the channel length direction in the center of fin body at V_{DS}=0.05 V and V_{GS}=V_{th} condition.

The empirical ($x_h^{'}$)s for an N_{b} of 5×10^{18} cm^{-3} was also obtained by the same manner. Empirical equation (2) and $x_h^{'}$ extracted from the simulated data are compared in Fig. 7 which shows $x_h^{'}$ versus W_{fin} as a parameter of L_{g} for the devices with N_{b}s of 2×10^{18} cm^{-3} and 5×10^{18} cm^{-3}. The V_{th} model of ideal DG bulk FinFETs was already derived by B-K. Choi *et al.* [6]. We took V_{th} model reflecting only DG nature, and changed charge-sharing term by considering barrier lowering as given by

$$V_{th} = V_{FB} + 2\psi_B + \delta_w + \frac{qN_b x_{dep}}{C_{ox}}\left(1 - \frac{x_h^{'}}{L_c}\right) \qquad (3)$$

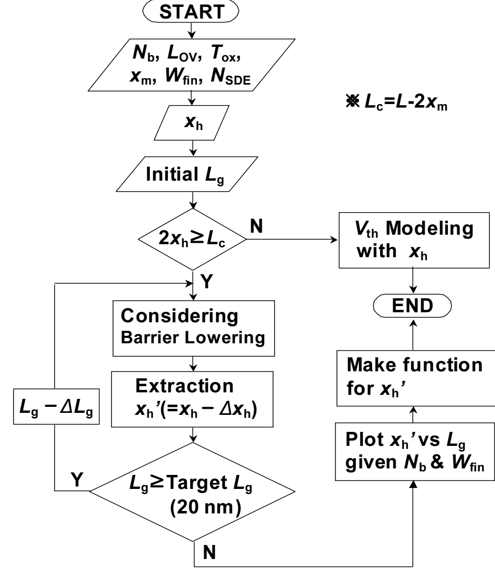

Fig. 6. Procedure of V_{th} modeling and extraction of chare-sharing length ($x_h^{'}$) depending on L_{g} for a DG MOSFET. Here, x_{m} is a parameter regarding box type channel doping and is calculated for a channel doping profile.

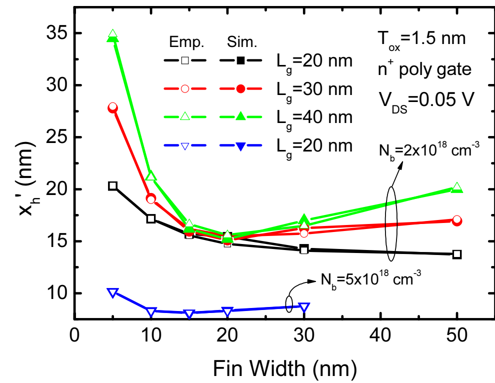

Fig. 7. $x_h^{'}$ versus W_{fin} as a parameter of L_{g} for the devices with N_{b}s of 2×10^{18} cm^{-3} and 5×10^{18} cm^{-3}. The empirical equations (open symbols) show a good agreement with ($x_h^{'}$)s from simulation (solid symbols).

where x_{dep} is a depletion width, and 0.5·W_{fin} if the fin body is depleted fully. The V_{FB}, 2ψ_{B} and C_{ox} are workfunction difference, surface potential at V_{th}, and gate oxide capacitance, respectively. We ignore oxide charge in this paper to simplify the modeling and simulations.

Fig. 6 shows the procedure of V_{th} modeling and extraction of suitable charge-sharing length ($x_h^{'}$) depending on L_{g} at a given N_{b} and W_{fin} for DG MOSFETs. Here, L_{c}(=L–2x_{m}) [6] is the channel length based on the box channel doping profile. L_{ov} is shown in Fig. 2.

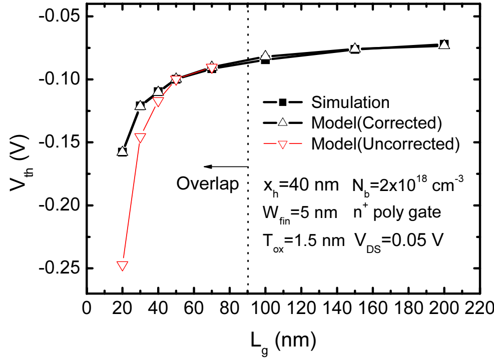

Fig. 8. V_{th} versus L_g. Here, W_{fin} of 5 nm and N_b of 2×10^{18} cm^{-3} are applied. The overlap of x_h occurs at L_g of 90 nm. The model(Corrected) shows a good agreement with 2-D device simulation.

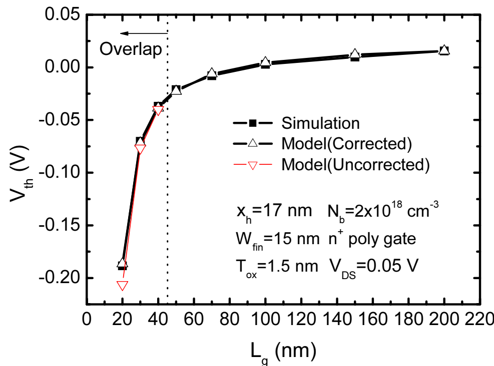

Fig. 9. V_{th} versus L_g. Here, W_{fin} of 15 nm and N_b of 2×10^{18} cm^{-3} are applied. The overlap of x_h occurs at L_g of 45 nm. The model(Corrected) shows a good agreement with 2-D device simulation.

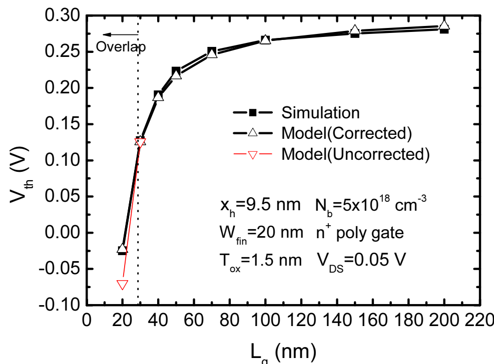

Fig. 10. V_{th} versus L_g. Here, W_{fin} of 20 nm and N_b of 5×10^{18} cm^{-3} are applied. The overlap of x_h occurs at L_g of 29 nm. The model(Corrected) shows a good agreement with 2-D device simulation.

Figs. 8 – 12 show V_{th} versus L_g at given W_{fin} and N_b. In these figures, charge-sharing length is overlapped in the left side of the dotted line. The V_{th} model of DG MOSFETs with the uncorrected x_h shows some error with 2-D device simulation for various conditions in the

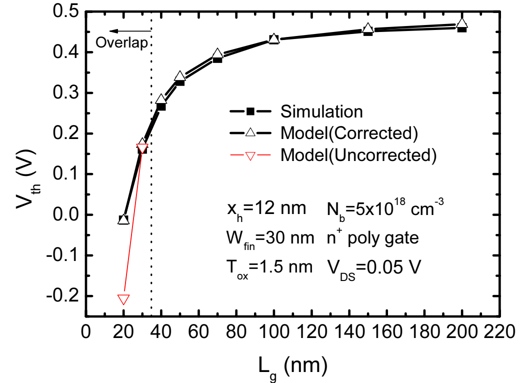

Fig. 11. V_{th} versus L_g. Here, W_{fin} of 30 nm and N_b of 5×10^{18} cm^{-3} are applied. The overlap of x_h occurs at L_g of 35 nm. The model(Corrected) shows a good agreement with 2-D device simulation.

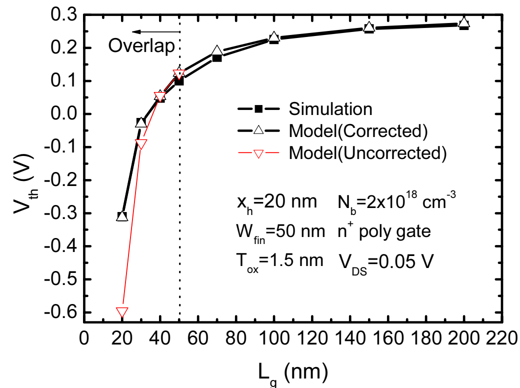

Fig. 12. V_{th} versus L_g. Here, W_{fin} of 50 nm and N_b of 2×10^{18} cm^{-3} are applied. The overlap of x_h occurs at L_g of 41 nm. The model(Corrected) shows a good agreement with 2-D device simulation.

overlapped channel length. But the V_{th} model of DG MOSFETs with the corrected x_h shows a good agreement with 2-D device simulation regardless of L_g, W_{fin}, and N_b.

IV. Conclusion

We have modeled threshold voltage (V_{th}) of double-gate (DG) MOSFETs by considering barrier lowering in the short channel devices. The barrier lowering was reflected in charge-sharing length (x_h) which was given by empirical equation including effects from fin body width and channel length. In V_{th} modeling, a fitting parameter δ_w which is a kind of empirical equation based on various data was introduced for higher accuracy. The V_{th} model was verified by comparing with 2-D simulation data for various fin body width, gate length, and fin body doping. Our compact model explained well

the V_{th} behavior when charge-sharing length is overlapped.

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