

Editorial



A 90nm CMOS process is now widely used for the mass production of digital CMOS chips. A 45nm process is expected to be commercially used within a couple of years. The supply voltage is also scaled down, but not as fast as expected. It is almost fixed at 1V, mostly because the threshold voltage cannot be scaled down as desired due to the leakage power limitation. In the nano-meter CMOS era, the high-gain and high-precision analog circuits are extremely difficult to be integrated on the same chip with digital circuits. The analog circuits will suffer from the voltage headroom problem, as the supply voltage is reduced. Also, the gate and subthreshold leakage currents cause the signal distortions, because the magnitude of leakage current is signal dependent. To overcome these problems, some analog functions such as PLLs are implemented with digital circuits. Also, a multi-stage OP amp and an OP-amp-less analog circuit are being developed to alleviate these problems.

In this special issue on “Analog Circuits for Nanometer CMOS”, six papers are presented to address some of the above-mentioned issues. The 1st paper shows the state-of-the art circuit design issues for low-voltage low-power DRAMs. The 2nd paper deals with the gate leakage and supply noise problems of PLL with a 32nm predictive CMOS model. The 3rd paper presents a systematic design guide of the nested Gm-C frequency compensation for a 3-stage CMOS OP amp. The 4th paper shows a 5GS/s 5-bit 113mW flash-type analog-to-digital converter with a 1V supply voltage at 0.13 μ m. The 5th paper presents a low power output driver circuit for multi-standard physical layer using a voltage mode driver and a current source. The 6th paper shows a noise suppression circuit for the reference voltage ladder of high-speed flash ADC using a transmission gate RC filter.

We would like to thank all the authors who submitted their excellent papers to this special issue.

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Special Issue Editor

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