Analysis of Subthreshold Behavior of FinFET using Taurus

Balasubramanian Murugan*, Samar K. Saha, and Rama Venkat***

***Abstract*—This paper investigates the subthreshold behavior of Fin Field Effect Transistor (FinFET). The FinFET is considered to be an alternate MOSFET structure for the deep sub-micron regime, having excellent device characteristics. As the channel length decreases, the study of subthreshold behavior of the device becomes critically important for successful design and implementation of digital circuits. An accurate analysis of subthreshold behavior of FinFET was done by simulating the device in a 3D process and device simulator, Taurus. The subthreshold behavior of FinFET, was measured using a parameter called S-factor which was obtained from the ln(I_{DS}) - V_{GS} characteristics. The value of S-factor of devices of various fin dimensions with channel length L_g in the range of 20 *nm* - 50 *nm* and with the fin width T_{fin} in the range of 10 *nm* - 40 *nm* was calculated. It was observed that for devices with longer channel lengths, the value of S-factor was close to the ideal value of 60 *mV/dec*. The S-factor increases exponentially for channel lengths, $L_g < 1.5\ T_{fin}$. Further, for a constant L_g, the S factor was observed to increase with T_{fin}. An empirical relationship between S, L_g and T_{fin} was developed based on the simulation results, which could be used as a rule of thumb for determining the S-factor of devices.**

***Index Terms*—FinFET, Tarus, subthreshold, S-factor**

Manuscript received May 10, 2006; revised Dec. 13, 2006.
* Department of Electrical and Computer Engineering, University of Nevada Las Vegas, NV 89154-4026
** Synopsys, Inc. Mountain View CA-94043
E-mail : venkat@egr.unlv.edu

I. INTRODUCTION

Scaling of Complementary Metal Oxide Semiconductor (CMOS) devices has provided one of the basic means for improving the device density, speed, and power reduction in integrated circuits. However, scaling of conventional planar CMOS devices is gradually reaching its limit, and the need for an alternate MOSFET structure becomes inevitable. Of the several non-conventional planar MOSFET structures proposed by various researchers, the Fin Field Effect Transistor (FinFET) proposed by Hisamoto, *et.al.*[1] in 1998, is found to be a promising candidate for fabricating MOSFET devices below 0.1 μm technology.

When devices are scaled, for gate voltages less than the threshold voltage (V_{th}) of scaled devices, the leakage current flowing in the device is very high due to the decrease of gate control on the channel. The subthreshold behavior of a device is defined as the behavior of the device, when the applied gate voltage is less than the threshold voltage. Under subthreshold condition the current flowing through the device is not zero, because a small diffusion current flows through the device. The subthreshold behavior, which is a measure of the gate control on the channel, is measured using a parameter called S-factor, which is given by [2]:

$$S = 2.3 \times \left(\frac{\partial V_{GS}}{\partial \ln(I_{DS})} \right) (mV/dec) \quad (1)$$

A complete analysis of the subthreshold behavior of FinFET is possible by numerical simulation of FinFET using a 3D process and device simulator, Taurus [3]. Since FinFET is a 3D device, simulating FinFET in a 3D simulator Taurus is the most appropriate method for a

detailed analysis of subthreshold behavior of FinFET.

The objective of this paper is to explore the subthreshold behavior of FinFET with alternate material as gate electrode. In order to achieve this goal, FinFET devices with channel length (L_g) ranging from 20 *nm* to 50 *nm* and channel widths (T_{fin}) ranging from 10 *nm* to 40 *nm* were simulated. The subthreshold behavior was analyzed by extracting the S-factor from the inverse of the slope of the $\ln(I_{DS})$ - V_{GS} characteristics. From the S-factor values obtained from numerical simulations the effect of FinFET geometry on the subthreshold behavior of the device was analyzed. An empirical relationship between S-factor and device dimensions was proposed, from which the S-factor of devices with various fin dimensions can be determined. Process and device simulations of FinFET using Taurus 3D-simulation tool are presented in section II. Details of the analysis, results and discussions are presented in section III. Conclusions are in section IV.

II. SIMULATION PROCEDURE

1. Process Simulation

In order to analyze the subthreshold behavior of FinFET, a 3D structure of FinFET device was simulated using Taurus Process & Device simulation programs, respectively. The Taurus process simulation tool simulates the fabrication steps used to manufacture the semiconductor devices. The Taurus device simulation tool simulates the complete electrical characteristics of the device.

A process simulation procedure for a 50 *nm* channel length FinFET with a fin width of 30 *nm* and a fin height of 50 *nm* was presented in this section and the simulation procedure is the same for all device dimensions. The device symmetry of the FinFET structure in all three dimensions, i.e., source to drain, top to bottom, and left to right, was exploited and only one-quadrant of the full FinFET device structure was process simulated. Reflecting one quadrant of the device about appropriate mid-planes going through the center of the device, the other 3 quadrants were obtained which will complete the full device.

A p-type Si-substrate with a doping concentration of $1\text{x}10^{16}$ cm^{-3} was used as a starting material. On the Si-

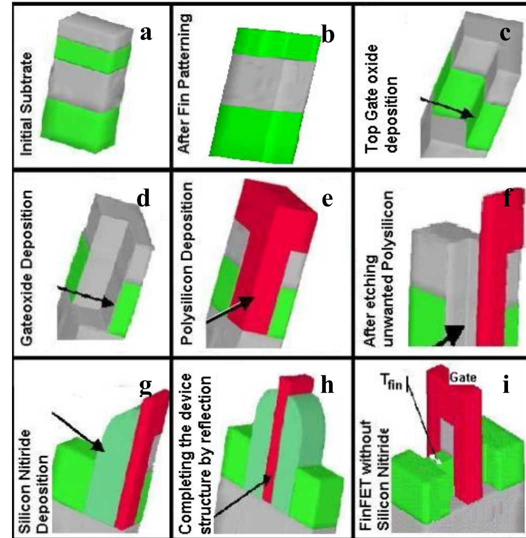

Fig. 1. 3 D view of the device structure at various steps in the process simulation of FinFET using Taurus process and device simulator. The sequence of processing steps follows (a) through (i).

substrate, a 100 *nm* buried oxide (BOX) was deposited followed by 50 *nm* thick Si. This forms the SOI substrate for the FinFET design with Fin height (H_{fin}) of 50 *nm*. In this analysis the fin height was kept a constant for all device dimensions. The 3D structure of the SOI substrate with masking oxide is shown in Fig. 1.a. The fin is patterned on the substrate and then, the masking oxide was then removed. A top gate oxide of thickness 40 *nm* and a back gate oxide of 1.5 *nm* were used for all device dimensions. After depositing the gate oxides, a layer of polysilicon was deposited. The unwanted polysilicon region was, then, etched. Subsequently, a layer of silicon nitride was deposited, which was used to prevent accidental implantation of the channel with source/drain implant. The unwanted silicon nitiride region covering the source/drain region was etched to expose the source/drain regions.

The n^+ source/drain regions with a dopant concentration of $2.71\text{x}10^{21}$ cm^{-3} were used. Sufficient time and temperature was given for Rapid Thermal Processing (RTP) so that the n^+ source/drain regions diffuse into the fin and overlap with the channel region under the gate. This overlap is necessary to avoid discontinuity of the channel at the source and drain end even after strong inversion of the channel. The already processed 3-D device structure has one quarter of the top gate, one half of the back gate and the source/drain is

shown in Fig. 1(b) Following the processing a quadrant of the FinFET, the complete 3-D structure of the FinFET device is formed by reflection about appropriate planes. The 3-D structure of a complete FinFET device structure with and without silicon nitride is shown in Fig. 1(c) and Fig. 1(d) respectively.

2. Device Simulation

In the deep sub-micron regime, the need for a mid-gap work function gate material becomes unavoidable. The energy band balance analysis for a MOSFET with a p-substrate and n^+ poly gate the metal-semiconductor work function difference, $\phi_{MS,}$ can be written as:

$$\phi_{MS} = \phi_M - (\chi_e + (E_g/2) - \phi_F) \quad (1)$$

where ϕ_M is the metal semiconductor work function, χ_e is the electron affinity of silicon, E_g is the energy band gap, and ϕ_F is the bulk potential. With $\phi_M = 4.05$ *eV*, $\chi_e = 4.1$ *eV*, and $E_g = 1.12$ *eV* (1) reduces to:

$$\phi_{MS} = - 0.56 - \phi_F \quad (2)$$

according to the scaling rule, as the devices are scaled, the concentration of the substrate increases. Consequently, $\phi_{MS} = 0$ *eV*, which implies that the device will be ON even when $V_{GS} = 0$ *V*. To overcome these problems, the use of mid band gap work function gate material becomes necessary [4]. When a gate material with a higher gate work function is used, i.e., $\phi_{MS}>0$, the device will not be ON at $V_{GS} = 0$ *V* and also the S-factor will be smaller. However, for replacing the polysilicon material, the material should be process-compatible with the earlier fabrication process, resistant to high temperature, and above all, it should have a mid-band gap work function.

Based on the contact resistance and ability to withstand temperature processing, nickel silicide was chosen as the material for the gate material. Depositing nickel metal on the polysilicon material and annealing it at ~600^oC forms a nickel silicide gate. Nickel mono silicide (NiSi) with a work function of 4.9 *eV* was used in this simulation. In this analysis, the FinFET device was process-simulated using the n^+ polysilicon material. During the device simulation, the work function of n^+ polysilicon material is replaced by the work function of the nickel silicide material to overcome the inability of the simulator to simulate the deposition of NiSi with a desired work function.

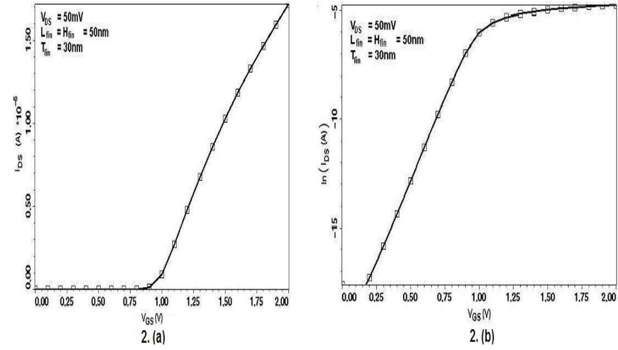

Fig. 2. I-V characteristics of the FinFET simulated using Taurus. (a) IDS versus VGS (b) ln(IDS) versus VGS.

With $V_{SUB} = 0$ *V* and $V_{DS} = 50$ *mV*, the gate voltage is ramped from 0 *V* to 1.5 *V* in increments of 0.1 *V*. The V_{th} and the subthreshold value are obtained from the program using the extract command. The I_{DS}-V_{GS} characteristics of a FinFET with channel length, $L_{fin} = 50$ *nm*, fin width, $T_{fin} = 30$ *nm*, and fin height, $H_{fin} = 50$ *nm*, with a drain bias, $V_{DS} = 0.05$ *V*, and gate bias, $V_{GS} = 1.5$ *V*, is shown in Fig. 2(a) $\ln(I_{DS})$ - V_{GS} characteristics obtained from the simulation are shown in Fig. 2(b)

III. Results and Discussion

From the I_{DS}-V_{GS} characteristics of a FinFET shown in Fig. 2(a), it is observed that the V_{th} of the device is high, i.e., $V_{th} = 0.78$ *V*. The reason for the high V_{th} is the high value of 4.9 *eV* used for the work function of nickel silicide. When materials with work function difference close to mid band gap work function are used as a gate, the V_{th} of the device will be high [5].

The S-factor, which is a measure of the subthreshold behavior of the device, is extracted from the $\ln(I_{DS})$-V_{GS} characteristics of the FinFET device. The S-factor of the above said device is found to be 67 *mV/dec*, which is close to the ideal S-factor of 60 *mV/dec*.

The S-factor for various channel lengths and widths for a constant fin height are obtained from the device simulation of FinFET. The fin height is found not to be a dominant parameter, and will not affect the depletion capacitance or the current flowing through the device, because the band bending from source to drain remains

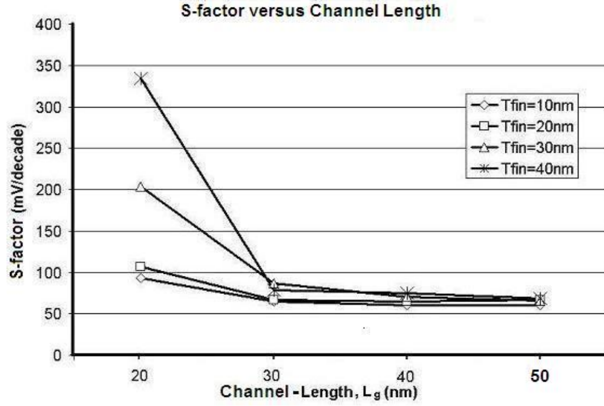

Fig. 3. S-factor versus fin length (Lg) of FinFET with various fin thicknesses, Tfin, obtained using Taurus.

the same even for different fin heights. The fin height and the gate oxide thickness are kept constant in this analysis. The fin width T_{fin} is in the range of 10 *nm* to 40 *nm* and the channel length L_g is in the range of 20 *nm* to 50 *nm*. A plot of S-factor versus channel length (L_g) for various fin widths is shown in the Fig. 3. It is observed that for a constant channel width, the S-factor increases exponentially with decreasing channel length. This exponential rise decreases with increasing fin thickness. For a longer channel length FinEFT device, the S-factor is close to the ideal value of 60 *mV/dec* and for these longer channel length devices, the increase in channel thickness does not increase the S-factor significantly.

Based an exhaustive trial and error method, an empirical formula relating the S-factor to the chanel length, L_g, and fin width, T_{fin}, of the form:

$$S = 60+K_1\exp\left(-K_2\frac{L_g}{\sqrt{T_{fin}}}\right) \quad (3)$$

was obtained for T = 300*K*. Two points from the simulation data were used to obtain K_1 and K_2. The values of K_1 and K_2 obtained from fitting the curves are 19926.58 *mV/dec* and -1.3539 $nm^{-1/2}$, respectively. The S-factor of devices with fin widths in the range of 10 *nm* to 40 *nm* are compared with the S-factor calculated using the empirical relation (3). In Fig. 4, the agreement between the results is fairly good and is within 20% for most cases. A plot of S-factor versus $\frac{L_g}{\sqrt{T_{fin}}}$ is shown in Fig. 5, which indicates that the S-factor obtained from the Taurus simulation and the empirical equation (3) agree

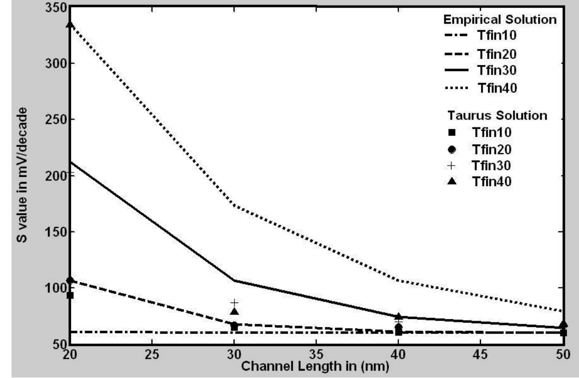

Fig. 4. Comparison of S-factor versus channel length obtained from Taurus simulation and empirical solution of Eq. 3. for various channel thicknesses.

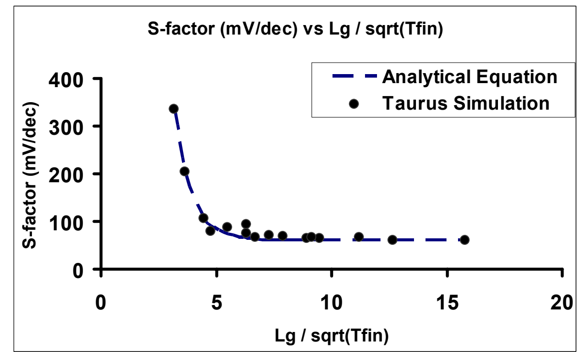

Fig. 5. Comparison of S-factor versus scaled channel length obtained from Taurus simulation and empirical solution for various channel thicknesses.

fairly well in most cases. Based on this empirical relationship, given a device dimension, one can calculate the S-factor of the device. Thus, this empirical equation can be used as a rule of thumb for device design.

IV. CONCLUSIONS

Simulating the FinFET device in Taurus device simulator does a detailed numerical analysis of the subthreshold behavior of FinFET. In this analysis, nickel silicide is used as a gate. The S-factor is obtained from the inverse of the slope of the $\ln(I_{DS})$-V_{GS} characteristics for various fin dimensions with the channel length L_g in the range of 20 *nm* - 50 *nm* and with the fin width T_{fin} in the range of 10 *nm* - 40 *nm*. It is observed that the S-factor increases exponentially with decreasing channel length. The rate of the exponential rise increases with increasing the channel thickness. For devices with longer channel lengths, the value of S-factor is close to the ideal

value of 60*mV/dec*. From the simulated S-factor, an empirical relationship using S, L_g and T_{fin} is obtained. The S-factor calculated from the empirical relationship is in fairly good agreement (within 20%) with the S-factor obtained from the Taurus simulation. Hence, the proposed empirical relationship can be used as a rule of thumb in determining the S-factor for FinFET devices.

REFERENCES

[1] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20nm," *IEEE Trans. Electron Devices*, vol. 47 no: 12, pp. 2320 –2325, Dec. 2000.

[2] J.R. Brews, "Subthreshold Behavior of Uniformly and Nonuniformly Doped Long-Channel MOSFET," *Electron Devices, IEEE Transactions on*, vol. ED-26, no. 9, pp. 1282 –1291, Sep. 1979.

[3] Taurus, Version 2002.4, Synopsys Corp., Mountain View, CA, 2002.

[4] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E.H. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm P-Channel FinFET," *Electron Devices Meeting, 1999. IEDM Tech. Digest. International*, pp. 67-70, 5-8 Dec. 1999.

[5] Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, M. Sidorow, E. Zhao, J. Zhang, J. Chan, A. Marathe, and M.-R. Lin, "Nickel silicide metal gate FDSOI devices with improved gate oxide leakage," *Electron Devices Meeting, 2002. IEDM '02. Digest. International*, pp. 271 –274, 8-11 Dec. 2002.

Balasubramanian Murugan received his Bachelor of Engineering degree in electronics and communication engineering from Bharathidasan University in 1999 and the M.S degree from University of Nevada Las Vegas in 2002. He is currently working in PDF solutions Inc., San Jose, CA, and is currently working on deep submicrometer device modeling and characterization issues.

Samar K. Saha received the M.S degree in Engineering Management from Stanford University and Ph.D degree in Solid State Physics from Gauhati University, Guwahati, India. Dr. Saha worked as an Assistant Professor in Electrical Engineering Department at Southern Illinois University, Carbondale, IL, and Auburn University, Auburn, AL. Since 1984 he has worked in various positions for National Semiconductor Corporation, LSI Logic Corporation, Texas Instruments, Philips Semiconductors, and Silicon Storage Technology. He is an Associate Graduate Faculty in the Electrical and Computer Engineering Department at the University of Nevada, Las Vegas, NV and an Adjunct Professor in Electrical Engineering Department at Santa Clara University, Santa Clara, and CA. His research interests include nanoscale device and process architecture, Technology CAD, Compact modeling, and TCAD and R&D management. He has authored more than 70 research papers, holds four US patents, and offered tutorials/short-courses on compact modeling and Technology CAD. Dr. Saha is a senior member of IEEE and Distinguished Lecturer of Electron Devices Society (EDS). He was the head guest Editor of the Special Issue of *IEEE Transactions on Electron Devices* on "Advanced Compact Models and 45-nm Modeling Challenges." He is the Editor-In-Chief of *IEEE QuestEDS*, chair of IEEE-EDS Compact Modeling Technical Committee, Vice-chair of EDS SRC-NAW, member of EDS-publications committee, EDS representative to the Council of Electronic Design Automation(CEDA), and the Vice-chair of Santa Clara Valley chapter of IEEE-EDS.

Rama Venkat received his B.Tech. from Indian Institute of Technology, Madras in 1983. He received his M.S. and Ph.D. degrees from Purdue University, West Lafayette, IN, in 1985 and 1988, respectively. He has been on the faculty of Electrical and Computer Engineering, University of Nevada, Las Vegas since 1989. He is currently a full professor in the department. He has over 35 journal articles covering processing and device physics, engineering and modeling. His current interests are in physics and modeling of nano-Si flash memories and SONOS.