

# Fabrication and Electrical Properties of Local Damascene FinFET Cell Array in Sub-60nm Feature Sized DRAM

Yong-Sung Kim\*, Soo-Ho Shin\*\*, Sung-Hee Han\*\*, Seung-Chul Yang\*\*,  
Joon-Ho Sung\*\*, Dong-Jun Lee\*\*, Jin-Woo Lee\*\*, and Tae-Young Chung\*\*

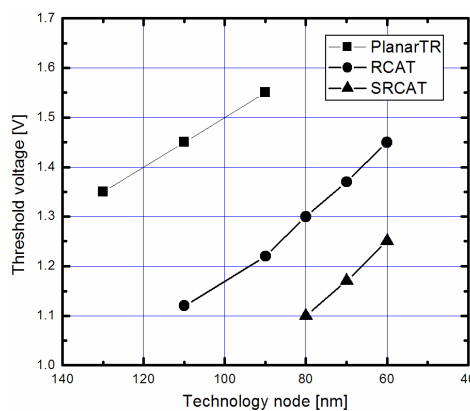
**Abstract**—We fabricate local damascene FinFET cell array in sub-60nm feature sized DRAM. The local damascene structure can remove passing-gate-effects in FinFET cell array. *p+* boron *in-situ* doped poly-silicon is chosen for the gate material, and we obtain a uniform distribution of threshold voltages at around 0.7V. Sub-threshold swing of 75mV/d and extrapolated off-state leakage current of 0.03fA are obtained, which are much suppressed values against those of recessed channel array transistors. We also obtain a few times higher on-state current. Based on the improved on- and off-state current characteristics, we expect that the FinFET cell array could be a new mainstream structure in sub-60nm DRAM devices, satisfying high density, low power, and high-speed device requirements.

**Index Terms**—FinFET, local damascene, cell transistor, threshold voltage, channel doping, passing gate effect, *p+* poly-silicon, low power DRAMs

## I. INTRODUCTION

As transistor size shrinks down, two-dimensional transistors face high off-state leakage current ( $I_{off}$ ). Necessarily, high threshold voltage ( $V_{th}$ ), low on-state

current ( $I_{on}$ ), and high channel doping concentrations become the major difficulties. Fig.1 shows the trend of threshold voltages for less than 1fA  $I_{off}$  as a function of device feature sizes. Because of the short channel effect (SCE) of planar cell transistors, the threshold voltages increase very steeply. Recessed channel array transistors (RCAT) [1] and spherical-RCAT (SRCAT) [2] reduce structurally SCE, and they have been adopted in DRAM cell with reduced channel doping concentrations.



**Fig. 1.** Trend of threshold voltages of the cell transistor according to technology node.

**Table 1.** Estimated cell transistor currents are listed for RCAT, as a function of device feature sizes and operating voltages. The  $V_{th}$  is assumed to be 1.25V, and the current values are in unit of  $\mu A/cell$ .

Design Rule	Operating Voltages		
	1.8V	1.5V	1.2V
90nm	3.01	1.08	0.12
80nm	2.62	0.94	0.11
70nm	2.29	0.83	0.1
60nm	1.96	0.73	0.08

Manuscript received Apr. 15, 2006; revised May 28, 2006.

\* Korea Research Institute of Standard and Science, Doryongdong, Yuseong-Gu, Daejeon, 305-600, Korea

\*\* Advanced Technology Development, Semiconductor R&D Center, Samsung Electronics Co., Ltd., San#24, Nongseo-Dong, Giheung-Gu, Yongin-City, Gyunggi-Do, 449-711, Korea

E-mail : godshin@samsung.com

Nevertheless,  $V_{th}$  of RCAT and SRCAT is still too high to operate in low voltage, and the  $V_{th}$  should be even higher as device size shrinks down. Table 1 summarizes estimated cell transistor currents as a function of feature sizes and operating voltages for RCAT structure. When the current is about 3 $\mu$ A/cell in 90nm feature size in 1.8V operation, the current is reduced down to almost zero in 60nm in 1.2V.

There have been a few reports on FinFET cell array for DRAM; FinFET cell array in sub-100nm trench capacitor DRAM [3], FinFET cell array with negative word line operation [4], and damascene FinFET cell array structure with local channel implantation scheme [5] for sub-60nm technology node. Since FinFET cell array structurally has low  $I_{off}$ , it can achieve low  $V_{th}$ , high  $I_{on}$ . However,  $V_{th}$  control is still an issue in thin body transistors, and a newly found passing-gate-effect in FinFET array has become another problem in the application of FinFET on DRAM cell [6].

In this paper, we report fabrication and electrical properties of FinFET cell array in sub-60nm feature sized DRAM.  $V_{th}$  of 0.7V is obtained with  $p^+$  boron *in-situ* doped poly-silicon gate, and, with the sub-threshold swing of 75mV/d, the extrapolated  $I_{off}$  is obtained lower than 0.03fA. Almost zero body effect is found in FinFET,

and the  $I_{on}$  of a few times higher than SRCAT is obtained.

## II. FABRICATION PROCESS

Fig. 2 shows major process sequence for local damascene FinFET cell array. Process sequence is as following. After active patterning and STI gap fill process, contact type is patterned on field oxide such as shown Fig. 3(a)(b). Sequentially, field oxide is etched

- Active patterning & STI gap fill process
- Local contact patterning
- $Si_3N_4$  deposition
- Chemical mechanical polishing
- Damascene patterning
- Gate oxide growth
- P+ poly/W/  $Si_3N_4$  deposition
- NMOS region open photolithography
- N+Poly(Ph.) doping
- Gate patterning
- Gate spacer & ILD process
- Contact process
- Metal formation

Fig. 2. Major process sequences for local damascene FinFET cell array.

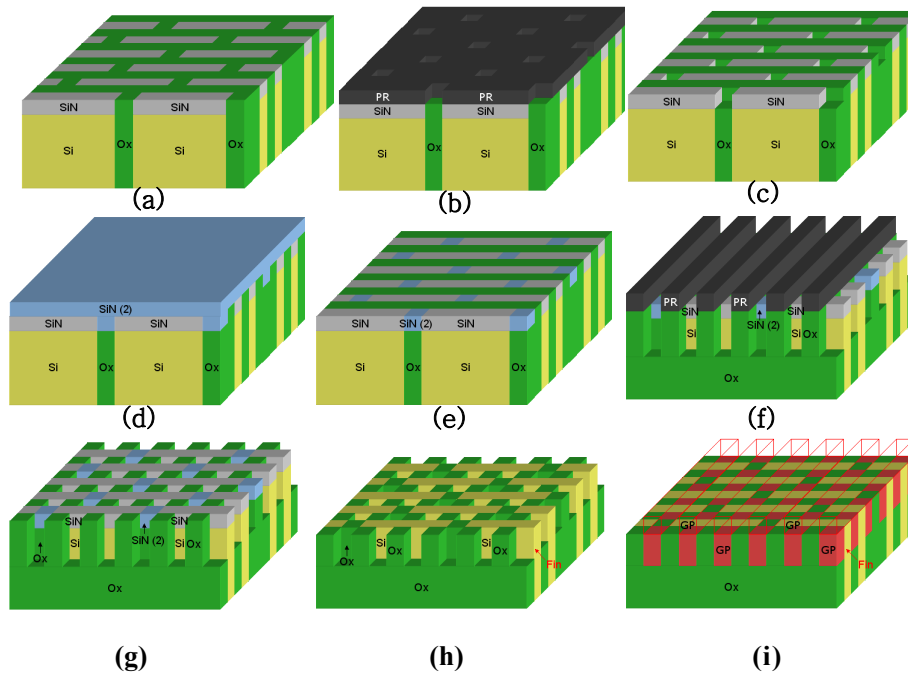
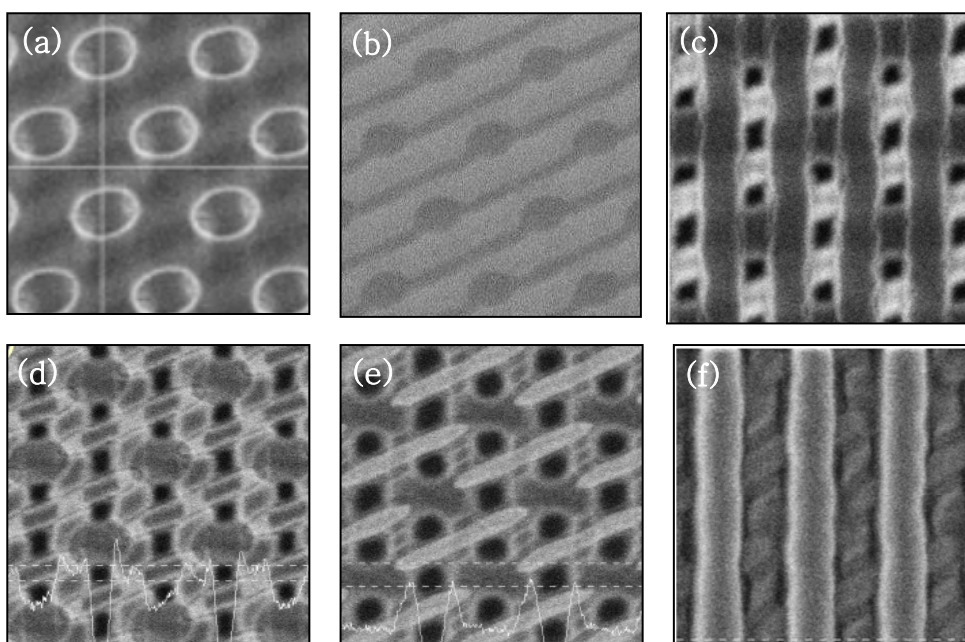


Fig. 3. Process schematics for FinFET cell array with local damascene pattern. (a) active/STI process, (b) local contact patterning on field oxide, (c) oxide etching, (d)  $Si_3N_4$  deposition, (e) CMP process, (f) damascene patterning, (g) field oxide etching, (h)  $Si_3N_4$  strip and (i) gate patterning.

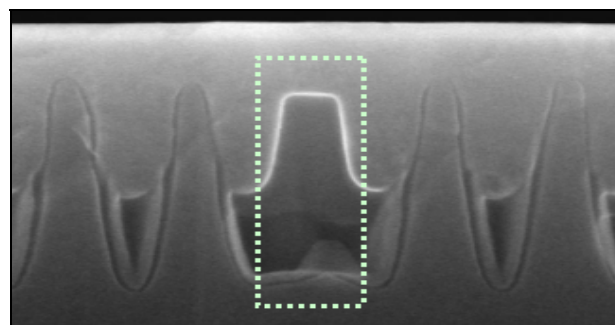


**Fig. 4.** Top views of cell array (a) after local contact pattern, (b)  $\text{Si}_3\text{N}_4$  CMP process, (c) damascene patterning, (d)  $\text{Si}_3\text{N}_4$  strip, (e) gate oxide growth and (f) gate patterning.

between two actives along their longer axis. Then  $\text{Si}_3\text{N}_4$  layer is deposited and we perform CMP process to form plugged  $\text{Si}_3\text{N}_4$  layer on these specific field regions. These specific field regions will be the passing gate locations. On this planarized surface, we do line and space photolithography and perform damascene etch process such as shown Fig. 3(f)(g). Next, the  $\text{Si}_3\text{N}_4$  masks are removed and the gate lines are patterned using conventional gate processes.

Fig. 4 shows the fabricated local damascene FinFET structure in sub-60nm feature size. Fig. 4(a) shows the contact type patterns after the field oxide etch process. The (b) image is after  $\text{Si}_3\text{N}_4$  CMP process. We can see the plugged  $\text{Si}_3\text{N}_4$  layers on the specific field regions. The (c) and (d) images show the damascene patterning and  $\text{Si}_3\text{N}_4$  strip process, respectively. At the both sides of an active, on where a gate shall run, the fields are not recessed for plugged  $\text{Si}_3\text{N}_4$  layer. The local damascene FinFET structure should be distinguished from conventional or damascene FinFET structures [6]. We use a combined process of a contact-type plugged  $\text{Si}_3\text{N}_4$  mask scheme and a line-and-space damascene etching scheme. Fig. 4(f) shows the cell array structure after gate formation. Boron *in-situ* doped  $p^+$  type poly-silicon is used for the gate material. For periphery NMOS, phosphorus is counter-doped on the deposited boron doped poly-silicon. Fig. 5 shows a vertical view of the

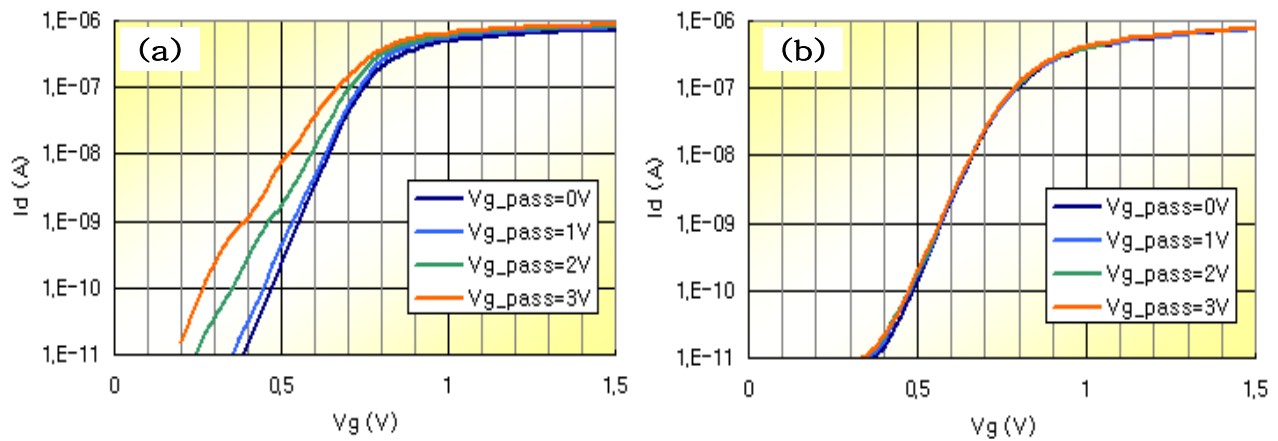
local damascene FinFET structures. There are two actives between not recessed field oxides. And so the passing gate is not recessed. In this paper, the fin width is about 30nm, the fin height is about 1000 Å, and the gate length is about 45nm on top, while it is longer at the fin sidewalls of about 60nm.



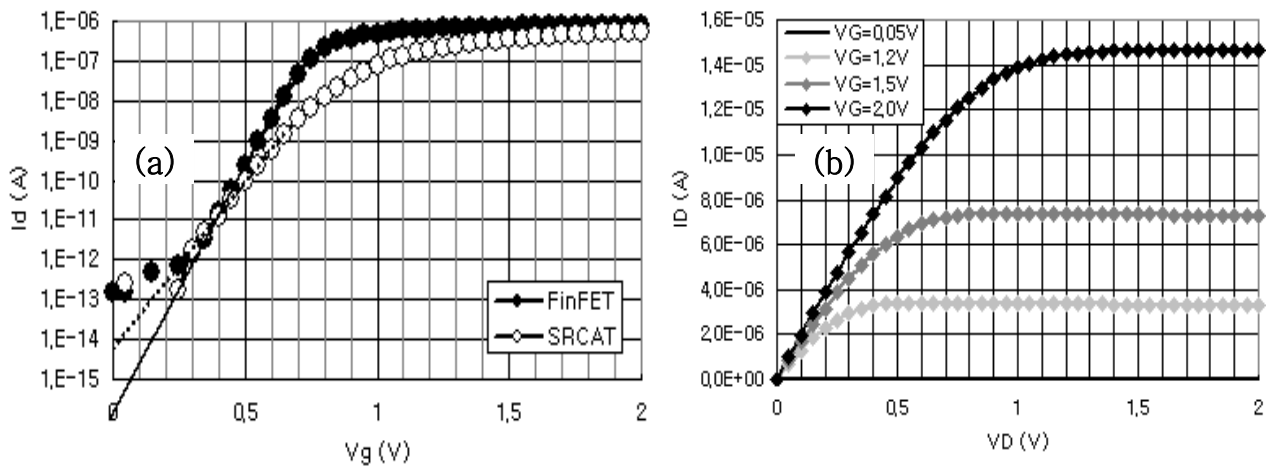
**Fig. 5.** Vertical SEM images of the local damascene FinFET structures after gate poly-silicon deposition.

### III. RESULTS AND DISCUSSION

Fig. 6 shows that the electrical result of the local damascene FinFET structure is compared with the damascene FinFET structure. The sub-threshold degradation which is severe in the damascene FinFET structure is not shown in the local damascene FinFET structure. The  $V_g$ - $I_d$  curves are almost identical



**Fig. 6.** Comparison of  $V_g$ - $I_d$  curve between (a) damascene and (b) local damascene FinFET structures according to passing gate biases.



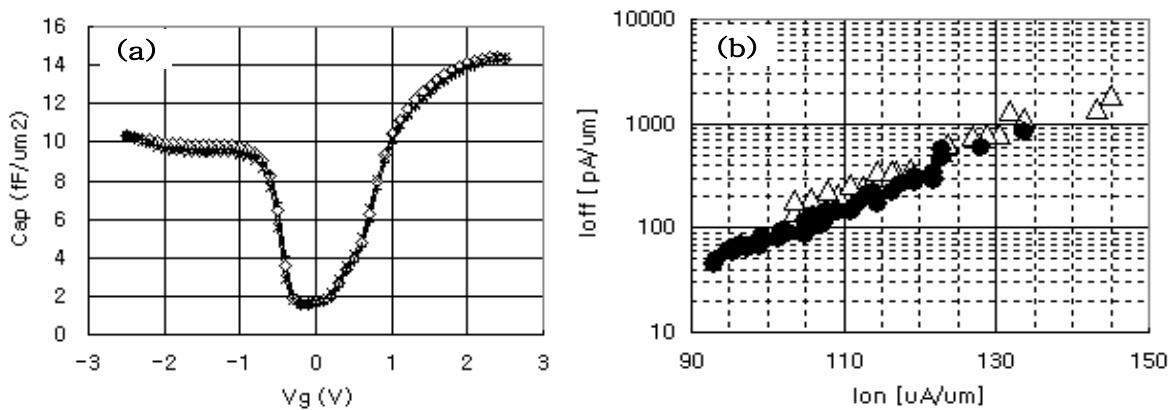
**Fig. 7.** (a)  $V_g$ - $I_d$  curves for SRCAT and FinFET and (b)  $V_d$ - $I_d$  curves for FinFET in sub-60nm feature size are compared

**Table 2.** Electrical properties of SRCAT and FinFET are compared in a wafer.

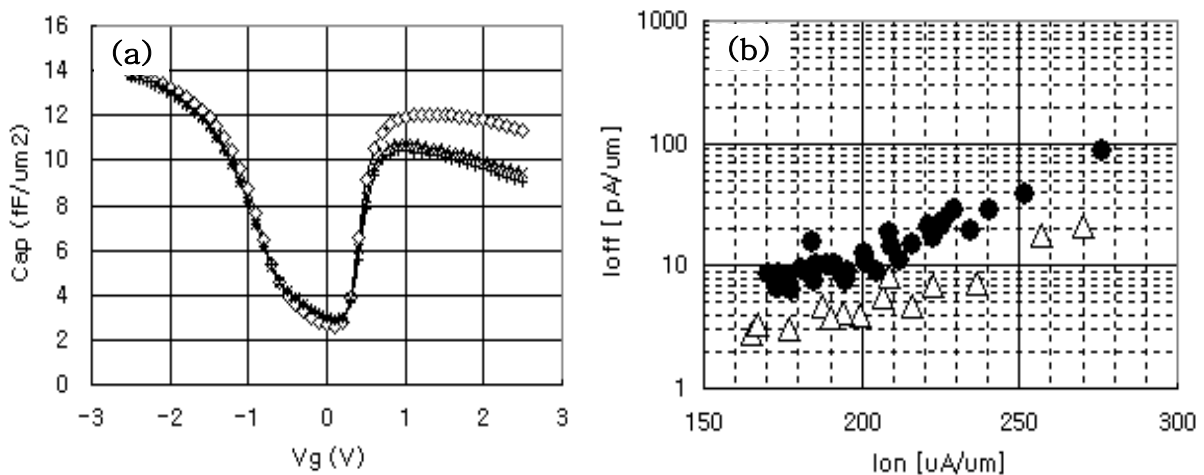
ITEM	SRCAT	FinFET
$V_{th}$	<b>0.7V</b>	<b>0.68V</b>
$\Delta V_{th}$	<b>400mV</b>	<b>200mV</b>
$I_{on}$	<b>1.2uA/cell</b>	<b>4.9uA/cell</b>
Swing	<b>110mV/d</b>	<b>75mV/d</b>
Body effect	<b>450mV</b>	<b>10mV</b>
DIBL	<b>20mV</b>	<b>20mV</b>

independent of the passing gate biasing. The passing gate potential is found to be electrically shielded by the storage node region. Fig. 7 shows  $V_g$ - $I_d$  curves for SRCAT and FinFET in the same feature sizes of sub-60nm. Sub-threshold swing is 75mV/d for FinFET,

which is much lower than 110mV/d of SRCAT. Correspondingly, extrapolated  $I_{off}$  at  $V_g=0V$  is of an order of 0.03fA in FinFET, while it is about 8fA in SRCAT. Threshold voltage is about 0.7V for FinFET, which is even lower than that of SRCAT (0.8V). For the similar  $I_{off}$  value of sub-fA, SRCAT needs higher  $V_{th}$ . Table 2 summarizes the differences in electrical properties between SRCAT and FinFET in a wafer. Body effect is reduced to almost zero in FinFET.  $I_{on}$  currents are about 4 times higher in FinFET. However, in the same  $I_{off}$  condition, the difference in  $I_{on}$  becomes even larger. Variation of  $V_{th}$  is also improved in FinFET cell array, as compared to SRCAT. The range of  $V_{th}$  in a wafer is about 200mV for FinFET, while it is around 400mV for SRCAT. Gate work function of  $p^+$  boron *in-situ* doped poly silicon determines the  $V_{th}$  of FinFET. Since we minimize the channel doping concentrations, the  $V_{th}$  is not sensitive to



**Fig. 8.** (a) C-V curve and (b) Ion-Ioff correlation curve of PMOS transistors in periphery region. The closed symbols are for the conventional  $n+$  doped poly-silicon with  $p+$  counter doping scheme, and the open symbols are for the simple  $p+$  doped poly-silicon scheme.



**Fig. 9.** (a) C-V curve and (b) Ion-Ioff correlation curve of NMOS transistors in periphery region. The closed symbols are for the conventional  $n+$  doped poly-silicon scheme, and the open symbols are for the  $p+$  doped poly-silicon with  $n+$  counter doping scheme.

the fin thickness variations. Reduced SCE in FinFET also reduces the dependency of  $V_{th}$  on fin height and gate length variations. Here, we set  $V_{th}$  be around 1.3V for SRCAT for similar  $I_{off}$  to FinFET.

When we compare the conventional  $p+$  counter doping scheme in  $n+$  doped poly-silicon and the simply  $p+$  doped poly-silicon scheme, we could not find any significant differences for PMOS transistors, as shown in Fig. 8. For NMOS transistors, we find that the inversion capacitances can be higher in  $p+$  doped poly-silicon with  $n+$  counter doping case than the conventional  $n+$  doped poly-silicon case. Counter doping scheme with  $n+$  dopant in  $p+$  doped poly-silicon gate has no difficulty in the type conversion, and we find the even improved NMOS transistor performances. Fig. 9(b) shows the increased  $I_{on}$  in NMOS transistor with  $p+$  doped poly-

silicon with counter doping. The improvement is about 10%, which is similar to improvement of inversion capacitance of about 9.6% at the gate voltage of 2V.

## VI. CONCLUSIONS

We fabricate local damascene FinFET array in DRAM cells in sub-60nm feature size. With local damascene gate structures, severe passing gate effects in FinFET array are effectively removed. We adopt  $p+$  boron *in-situ* doped poly-silicon gate in cell array, and, as a result, very uniform distribution of threshold voltage are obtained. And  $I_{off}$  is found to be two orders of magnitude lower, as compared to SRCAT. In this  $I_{off}$  condition, we obtain  $I_{on}$  of 4 times higher than that of SRCAT. In

addition, we find that  $n+$  counter doping scheme in  $p+$  doped poly-silicon is also very applicable to NMOS transistor design. Based on the improved  $I_{on}$  and  $I_{off}$  characteristics, we expect that the FinFET cell array should be a new mainstream structure for sub-60nm DRAM devices, satisfying high density, low power, and high-speed device requirements.

## REFERENCES

- [1] J.Y. Kim, C.S. Lee, S.E. Kim, I.B. Chung, Y.M. Choi, B.J. Park, J.W. Lee, D.I. Kim, Y.S. Hwang, J.M. Park, D.H. Kim, N.J. Kang, M.H. Cho, M.Y. Jeong, H.J. Kim, J.N. Han, S.Y. Kim, B.Y. Nam, H.S. Park, S.H. Chung, J.H. Lee, J.S. Park, H.S. Kim, Y.J. Park and Kinam Kim, "The breakthrough in data retention time of DRAM using Recess-Channel-Array Transistor(RCAT) for 88nm feature size and beyond," *VLSI Technical Digest*, pp.11-12, 2003.
- [2] J.Y. Kim, H.J. Oh, D.S. Woo, Y.S. Lee, H.H. Kim, S.E. Kim, G.W. Ha, H.J. Kim, N.J. Kang, J.M. Park, Y.S. Hwang, D.I. Kim, B.J. Park, M. Huh, B.H. Lee, S.B. Kim, M.H. Cho, M.Y. Jung, Y.I. Kim, C. Jin, D.W. Shin, M.S. Shim, C.S. Lee, W.S. Lee, J.C. Park, G.Y. Jin, Y.J. Park, and Kinam Kim, "S-RCAT(Sphere-shaped-Recess-Channel-Array Transistor) Technology for 70nm DRAM feature size and beyond," *VLSI Technical Digest*, pp.34-35, 2005.
- [3] R. Katsumata, N. Tsuda, J. Idebuchi, M. Kondo, N. Aoki, S. Ito, K. Yahashi, T. Satonaka, M. Morikado, M. Kito, M. Kido, T. Tanaka, H. Aochi and T. Hamamoto, "Fin-Array-FET on bulk silicon for sub-100nm Trench Capacitor DRAM," *VLSI Technical Digest*, pp.61-62, 2003.
- [4] C.H. Lee, J.M. Yoon, C. Lee, H.M. Yang, K.N. Kim, T.Y. Kim, H.S. Kang, Y.J. Ahn, D.G. Park, and Kinam Kim, "Novel Body Tied FinFET Cell Array Transistor DRAM with Negative Word Line Operation for sub 60nm Technology and beyond," *VLSI Technical Digest*, pp.130-131, 2004.
- [5] C. Lee, J.M. Yoon, C.H. Lee, J.C. Park, T.Y. Kim, H.S. Kang, S.K. Sung, E.S. Cho, H.J. Cho, Y.J. Ahn, D.G. Park, Kinam Kim, and B.I. Ryu, "Enhanced Data Retention of Damascene-finFET DRAM with

Local Channel Implantation and  $\langle 100 \rangle$  Fin Surface Orientation Engineering," *IEDM*, pp.61-64, 2004.

- [6] Y.S. Kim, S.H. Lee, S.H. Shin, S.H. Han, J.Y. Lee, J.W. Lee, J. Han, S.C. Yang, J.H. Sung, E.C. Lee, B.Y. Song, D.J. Lee, D.I. Bae, W.S. Yang, Y.K. Park, K.H. Lee, B.H. Roh, T.Y. Chung, Kinam Kim, and Wonshik Lee, "Local-Damascene-FinFET DRAM Integration with  $p+$  Doped Poly-Silicon Gate Technology for sub-60nm Device Generations," *IEDM*, pp.325-328, 2005.



**Young-Sung Kim** received the Ph. D. in Physics from KAIST, Daejeon, Korea, in 2002. He joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea, from 2002 to 2006. He has been involved in the development of high-density DRAM with sub-100nm and sub-60nm feature sizes. He was specialized in 3D cell transistor technology, such as RCAT and FinFET. He recently joined Korea Research Institute of Standards and Science (KRISS). His current interest is atomic scale simulation of semiconductor materials and devices through the *ab initio* calculations.



**Soo-Ho Shin** received the B.S. and M.S. degrees in electronic engineering from Kookmin University, Seoul, Korea, in 1994 and 1996, respectively. In 1996, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea, where he has been involved in the development of high-density DRAM such as 1G DRAM and 4G DRAM. His current interests are sub-60nm memory cell technology and metal gate process.



**Sung-Hee Han** received the B.S. degrees in electronic engineering from Kwangwoon University, Seoul, Korea, in 2000. In 2000, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea,

where he has been involved in the development of high-density DRAM. His current interests are sub-60nm memory cell technology and metal gate process.



**Seung-Chul Yang** received the B.S. degrees in ceramic engineering from HanYang University, Seoul, Korea, in 2005.

In 2005, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea,

where he has been involved in the development of 512M DRAM with sub-60nm minimum feature size. His current interests are selective epitaxial growth (SEG) process and metal gate process.



**Joon-Ho Sung** received the B.S. and M.S. degrees in chemistry from Busan National University, Busan, Korea and , KAIST, Daejeon, Korea, in 2003 and 2005, respectively.

In 2005, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea, where he has been involved in the development of 512M DRAM with sub-60nm minimum feature size. His current interests are sub-60nm memory cell technology and metal gate process.



**Dong-Jun Lee** received the B.S. and M.S. degrees in chemical engineering from Sogang University, Seoul, Korea, in 1999, and 2001, respectively.

In 2001, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea, where he has been involved in the development of of high-density DRAM. His current interests are sub-60nm memory cell technology and metal gate process.



**Jin-Woo Lee** received the B.S, M.S degrees from KeyungPuk University, Daegu, Korea in 1993 and 1995, respectively.

In 1995, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyeonggi-Do, Korea, where he was engaged in Semiconductor Device Engineering Team, and was working on the MOS device physics and DRAM process technologies. He is currently working on sub-60nm DRAM product development.



**Tae-Young Chung** received the BS and MS degrees in physics from Yonsei University, Seoul, Korea, in 1983 and 1985, respectively. He also received the Ph.D. degree in physics from KAIST, Daejeon, Korea, in 1998. In January 1985 he joined

Samsung Electronics Co. Ltd., Gyeonggi-Do, Korea. He worked on the developments of 4Mb and 16Mb DRAMs between 1986 and 1993 as a member of process integration group. After the Ph.D. program he was involved in key technology developments and product applications using 140nm technology node from 1998 to 2001. Since 2002 he has been in charge of research group developing DRAM of deep sub-100nm technology nodes. His current interests are in high speed and low power DRAMs using new device structures and materials.