

Editorial



Semiconductor devices opened the door into the nanoelectronics era. In CMOS technology, the 100 nm channel length barrier, which once was considered as almost impenetrable, fell down years ago, and the progress is accelerating toward the era of 10 nm channel length. The alternatives to CMOS devices such as impact-ionization metal-oxide-semiconductor (IMOS) devices and single electron transistors (SETs) have also been rapidly developed. The eight papers of this issue provide exciting results on recent advancement in nanoscale semiconductor device research. The subjects of the papers include quantum effect modeling, novel materials and device structures, noise in nanoscale CMOS devices, and alternative devices.

The first paper describes a framework of quantum effect simulation. S. Jin *et al.* present the development of a simulation program which implements a top-down approach based on the macroscopic quantum correction model and a bottom-up approach based on the microscopic non-equilibrium Green's function formalism. The next four papers address material, fabrication, and device structure issues. M. Jang *et al.* have fabricated and characterized various sizes (from 20 μm to 10 nm) of erbium/platinum silicided *n/p*-type Schottky barrier metal-oxide-semiconductor field effect transistors. W. Cho demonstrates single channel and multi-channel p-type FinFET devices with a gate length of 20-100 nm by boron diffusion from poly-boron films. S. Kim *et al.* show highly manufacturable Multi-channel Field Effect Transistors (McFET) on bulk silicon substrates. C. Oh *et al.* propose and implement a partially insulated MOSFET (PiFET) structure and an 80 nm 512M DDR DRAM with partially-insulated cell array transistors (PiCATs). In the last paper on CMOS technology, J. Lee *et al.* report $1/f$ noise power spectrum density of sub-100 nm MOSFETs for various parameters such as hot carrier stress, bias condition, temperature, device size and types.

The last two papers describe alternative devices. W. Choi *et al.* demonstrate 80-nm self-aligned n- and p-channel I-MOS devices using double sidewall spacer, elevated drain structure and RTA process. S. Kim *et al.* have fabricated and characterized single-electron transistor (SET)-based logic cells and SET/FET hybrid integrated circuits on SOI substrates.

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Editor of nanoscale semiconductor devices special issue

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