

Editorial

Following the last year's tradition, JSTS 2005 December issue is a special issue on System-on-chip (SoC) Design. As the semiconductor manufacturing technology achieves the scales of 90nm and below, integration of practical systems on a chip becomes possible, reducing cost, power consumption, and physical size.

The 2005 International SoC Design Conference (ISOCC 2005) was held in Seoul Korea on October 20-21, 2005. The Technical Society of SoC Design of IEEK hosted this 2nd international event of information exchanges and productive discussions on the state of the art technology on all aspects of SoC design. Among the 120 papers presented at the conference, 9 outstanding papers have been invited for submission in this special issue.

The 1st paper proposes a fast and accurate power model of the ARM926EJ-S processor, focussing on the cache power model. The 2nd paper presents a system-level architecture evaluation technique to find performance bottleneck and to provide appropriate feedback. The 3rd paper proposes new instructions and hardware architecture for H.264/AVC. The 4th paper describes the embedded real-time software architecture for unmanned autonomous helicopter. The 5th paper presents a SoC design for digital TV. A single LSI incorporates processor, decoders, and analog IPs. In the 6th paper, the authors propose a new method for extracting inductance circuit models targeting for multiple-GHz SoC and SiP designs. The 7th paper describes a hierarchical flash memory based storage systems for enhanced access time and cost-effectiveness. The 8th paper presents a case study of Linux based smartphone hardware and software. Finally, the 9th paper presents a low voltage IF QPSK receiver block which consists of programmable gain amplifier and analog-to-digital converter.

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Guest Editor of the Special Issue



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