Analysis of 1/*f* Noise in Fully Depleted n-channel Double Gate SOI MOSFET

Alok Kushwaha, Manoj Kumar Pandey, Sujata Pandey, and A. K. Gupta

Abstract——**An analysis of the 1/*f* or flicker noise in FD n-channel Double Gate SOI MOSFET is proposed. In this paper, the variation of power spectral density (PSD) of the equivalent noise voltage and noise current with respect to frequency, channel length and gate-to-source voltage at various temperatures and exponent *C*(i.e 1/f^c) is reported. The temperature is varied 125 *K* from to room temperature. The variation of PSD with respect to channel length down to 0.1μm technology is considered. It is analyzed that 1/*f* noise in FD n-channel Double Gate SOI MOSFET is due to both carrier-density fluctuations and mobility-fluctuations. But controversy still exits to its origin.**

Index Terms——**Fully depleted, silicon-on-insulator, power spectral density**

I. Introduction

Silicon-on-insulator (SOI) MOS devices are given much attention owing to their advantages of higher circuit speed, lower power consumption, greater immunity to radiation induced errors and compatibility with existing IC fabrication process. Also, thinning of a silicon layer leads to the suppression of the short-channel effects [1].

The thin film double-gate SOI MOSFET has two gates simultaneously controlling the charge in the thin silicon layer, allowing two channels for current flow. This gives advantages over the single-gate SOI-MOSFET as drain current enhances considerably. The same gate-to-source voltage is applied on the both gate. Because FD SOI film is thin, invariably a direct charge coupling exists between the front and back gates [2]-[3].

It has so far been assumed that the drain current of a MOS transistor varies with time only if one or more of the terminal voltages vary with time. This is not exactly true. A careful examination of the current reveals minute fluctuations, referred to as noise, so ways to predict and possibly reduce noise are very important. For these reasons, the subject of noise in MOS transistors has received much attention. This paper is devoted to or flicker noise in double gate SOI-MOSFET, one of the main noise in MOS transistors.

Flicker noise in MOS transistors has been the subject of intense studies for several decades. There are several theories for the origin of this noise, which involved physics and sometimes-conflicting conclusions and several remaining unresolved issues [4]-[14]. The first theory relates the origin of flicker noise to the random fluctuation of the number of carriers in the channel, due to fluctuations in the surface potentials; the fluctuations are in turn caused by trapping and releasing of carriers by traps located near the Si-SiO2 interface [15]-[16]. It can be shown that a power spectral density nearly proportional to the inverse of the frequency results [17]-[18]. The effects discussed above can be thought of as randomly varying the effective interface charge density Q_0. This is equivalent to a noise voltage in series with the gate and proportional to $1/C_{ox}$; the mean square value of this noise is proportional to $1(C_{ox})^2$. $1/f$ noise results from the superposition of such variations due to many traps; the larger the gate area *WL*, the more the effects of these variations tend to average out,

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and the smaller the resulting noise.

A second theory attributes flicker noise to mobility fluctuations, due to carriers' interactions with lattice fluctuations [19]-[21]. Some research suggests that flicker noise is due to both carrier number fluctuations and mobility fluctuations [22]-[23]. After all, the carrier number fluctuation theory talks about a randomly varying charge at traps near the interface and it have been seen that charge can affect mobility through "coulombs scattering"; so it is not surprising that both effects may be present and correlated in a given device [24].

In this paper, we have shown the effect of flicker noise specifically in double gate SOI-MOSFET. For this first we have derived the current equation, transconductance, device capacitance, frequency and finally the Power Spectral Density of the equivalent noise voltage or current by taking the PEARSON-IV type distribution into account.

II. Theoretical Considerations

The cross-sectional view of double gate SOI-MOSFET is shown in Figure 1.

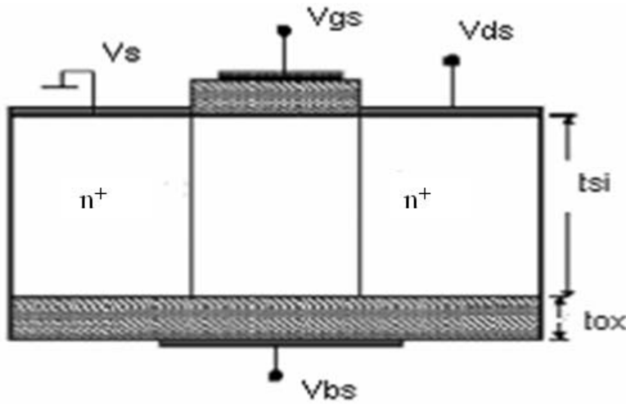

Fig. 1. Cross sectional view of double-gate SOI MOSFET.

The potential in the silicon film $\varphi(x, y)$ is obtained by solving Poisson's equation

$$\nabla^2\varphi(x,y) = \frac{qN_d^+(y)}{\varepsilon_{si}} \quad \text{for } 0 \le y \le t_{si},\ 0 \le x \le L \tag{1}$$

Where $N_d^+(y)$ is the ionized donor concentration, given by

$$N_d^+(y) = N_d(y)\left(1 - \frac{1}{\frac{1}{g}\exp\left[\left(E_d - E_f\right)/kT\right]}\right) \tag{2}$$

Where 'g' is the degeneracy factor and $N_d(y)$ represents the Pearson-IV-type doping distribution [25].

E_d, Donor ionization energy [26] $\quad \left(\frac{\varepsilon_o}{\varepsilon_{si}}\right)^2\left(\frac{m_{ce}}{m_o}\right)E_h \quad (3)$

E_f, Fermi energy [26] is given by,

$$E_f = kT\ln\left(\frac{N_d(y)}{n_i}\right) \tag{4}$$

Where is ε_0 the permittivity of the free space, m_{ce} is the conductivity effective mass of the electron, m_0 is the rest mass of an electron and E_h= 13.6 eV.
where is n_i the intrinsic carrier concentration and written as

$$n_i = 3.1\times10^{16}T^{\frac{3}{2}}\exp\left(\frac{-E_g}{2kT}\right) \tag{5}$$

E_g is the bandgap [27] given by

$$E_g = \left[1.16 - \left(\frac{7.02\times10^{-4}T^2}{1108+T}\right)\right]eV \tag{6}$$

The potential at the surface, $\varphi_s(x)$ and that at the center, $\varphi_s(x)$, of the SOI film [28] is given by

$$\varphi_s(x) = \frac{1}{1+\left(\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right)}\left(\varphi_c(x) + \frac{\varepsilon_{ox}\varepsilon_{si}V'_{gs}}{4\varepsilon_{si}t_{ox}}\right) \tag{7}$$

Where $V'_{gs} = V_{gs} - V_{fbf}$ (8)

Substituting $\varphi_s(x)$ from equation (7) in equation (1) we get

$$\frac{d^2\varphi_c(x)}{dx^2} - \left(\frac{\varphi_c(x) - V'_{gs}}{\lambda^2}\right) = \frac{qN_d^+(y)}{\varepsilon_{si}} \tag{9}$$

where λ is the natural length given as

$$\lambda = \left[\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}} \right) t_{si} t_{ox} \right]^{\frac{1}{2}} \tag{10}$$

Now making substitution - $\varphi_f(x) = \varphi_c(x) - V'_{gs} + \frac{qN_d^+(y)}{\varepsilon_{si}} \lambda^2$ (11)

In equation (9) and solving for potential distribution, we get

$$\varphi_f(x) = A \exp\left(\frac{-x}{\lambda} \right) + B \exp\left(\frac{x}{\lambda} \right) \tag{12}$$

Flatband voltage, V_{fbf} is given by

$$V_{fbf} = \frac{E_g}{2} - \phi_{bi} \tag{13}$$

where ϕ_{bi} is the built-in-potential

$$\phi_{bi} = \frac{E_g}{2} + \frac{kT}{q} \ln\left(\frac{N_d(y)}{n_i} \right) \tag{14}$$

Using equation (11) and (12), the potential at the center is given by

$$\varphi_c(x) = V'_{gs} - \frac{qN_d(y)}{\varepsilon_{si}} \lambda^2 + A \exp\left(\frac{-x}{\lambda} \right) + B \exp\left(\frac{x}{\lambda} \right) \tag{15}$$

Where A and B are the arbitrary constants and can be determined by using the following boundary conditions at the source and drain ends

$$\varphi_f(0) = \phi_{bi} - V'_{gs} + \frac{qN_d(y)\lambda^2}{\varepsilon_{si}} = \eta_s \qquad (x = 0) \tag{16}$$

$$\varphi_f(L_g) = V_{ds} + \phi_{bi} - V'_{gs} + \frac{qN_d(y)\lambda^2}{\varepsilon_{si}} = \eta_d \qquad (x = L_g) \tag{17}$$

For a strongly inverted doubled gate SOI MOSFET the current in the channel is given by

$$I_{ds} = W\mu_n(x) Q_n(x) \left(\frac{d\varphi_c(x)}{dx} \right) \tag{18}$$

where $Q_n(x)$ is the inversion layer charge given by

$$Q_n(x) = 2[Q_s(x) - Q_d(x)] \tag{19}$$

where $Q_n(x)$ and $Q_d(x)$ are the surface charge and depletion layer charge densities

$$Q_s(x) = -C_{ox} [V_{gs} - V_{fbf} - \varphi_c(x)] \tag{20}$$

where is C_{ox} the oxide capacitance given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{21}$$

and V_{fbf} is the flatband voltage, V_{gs} is the applied gate bias and $\varphi_c(x)$ is the channel potential

$$Q_d(x) = (2qN_d(x)\varepsilon_{si})^{\frac{1}{2}} (\varphi_s(x))^{\frac{1}{2}} \tag{22}$$

$\mu_n(x)$, the mobility of electron is given by

$$\mu_n(x) = \frac{\mu_{no}}{\left[1 + \left(E(x) / E_c \right)^2 \right]^{\frac{1}{2}}} \tag{23}$$

where μ_{no} is the low field mobility [29], E_c is the critical and $E(x)$ is the longitudinal field given by

$$E(x) = C_{ox} \frac{V_{fbf} - V_{gs} + \varphi_c(x)}{\varepsilon_{si}} \tag{24}$$

$$E_c = 6.01 \times 10^2 T^{3/2} \tag{25}$$

By substituting these components in equation (18), the equation for I_{ds}, drain to source current become[36]

$$I_{ds} = \frac{2W}{L_g} \mu_{no} E_c \varepsilon_{si} \left[\ln(P)(\varphi_s(x))^{1/2} - \frac{V_{ds}}{1 + L_g} + \ln(P)(V_{gs} - V_{fbf}) - V_{ds} \ln(P) + \ln(P)\varphi_c(x) \right] \tag{26}$$

$$\text{where } P = \frac{\varepsilon_{si} E_c + C_{ox}(V_{fbf} - V_{gs})}{\varepsilon_{si} E_c + C_{ox}(V_{fbf} - V_{gs} - V_{ds})}$$

Also, transconductance, $g_m = \left(\frac{\partial I_{ds}}{\partial V_{gs}} \right)_{V_{ds} = \text{cons}\tan t}$ (27)

Therefore the cut-off frequency, f is given by

$$f = \frac{g_m}{2\pi L_g W C_t} \tag{28}$$

where C_t is the total device capacitance per unit gate area(shown in the Figure 2) is given by

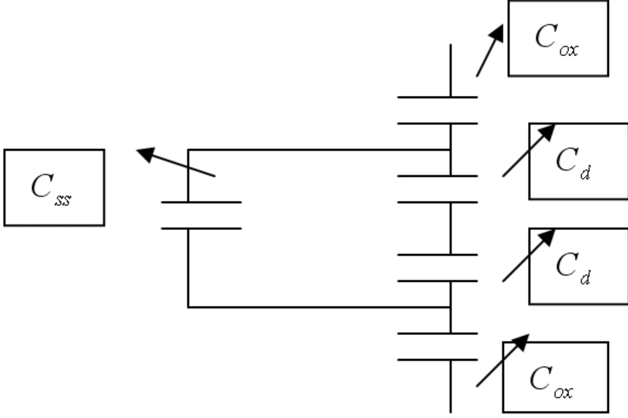

Fig. 2. Equivalent circuit for the device capacitance.

$$C_t = \frac{C_{ox}(C_{dp} + C_{ss})}{C_{ox} + 2(C_{dp} + C_{ss})} \tag{29}$$

where $C_{dp} = \frac{C_d}{2}$ and

$$C_d = \frac{\partial Q_d}{\partial V_{gs}} = \sqrt{\frac{qN_d(x)\varepsilon_{si}}{2\varphi_s(x)}}\frac{d\varphi_s(x)}{dV_{gs}} \tag{30}$$

and C_{ss}, the interface capacitance [31] is given by

$$C_{ss} = qN_{ss} \tag{31}$$

where N_{ss} is interface state density

Using detailed physical consideration, the power spectral density of the equivalent noise voltage can be shown as [32]-[34].

$$S_{vf}(f) = \frac{K_1}{C_{ox}^2 W L_g f^c} \tag{32}$$

where, for n-channel devices, the exponent varies between 0.7 and 1.2 and is a quantity independent of bias but depends on fabrication details, usually varies between 5×10^{-31}- 1×10^{-30} C^2 / cm^2.

Corresponding to this power spectral density of equivalent drain noise current can be shown as

$$S_{if}(f) = g_m^2 S_{vf}(f) \tag{33}$$

On the basis of second theory, flicker noise due to mobility fluctuation (due to carrier interaction with lattice fluctuations), the power spectral density for the equivalent noise voltage is [16],[19]-[21],[35]

$$S_{vf}(f) = \frac{K(V_{gs})}{C_{ox} W L_g f} \tag{34}$$

where $K(V_{gs})$is a bias dependent quantity, is of the order of 6×10^{-26} to 2×10^{-23} V^2F.

III. Results and Discussions

Figure 3 shows the variation of Noise Power Spectral Density with frequency and its comparison with experimental data[37]. By varying channel length L_g up to $0.3\mu m$ thereby the size (WL) and exponent from 0.70 to 1.00 keeping others fixed, it is seen that noise power spectral density is $\left(\frac{V^2}{Hz}\right)$ decreasing with increasing value of frequency (1GHz-120GHz). This is because of reduced trap charges act less effect of hot carriers electrons on the oxide layer in case of double gate SOI MOSFET. Curve having squares is at lesser value of c

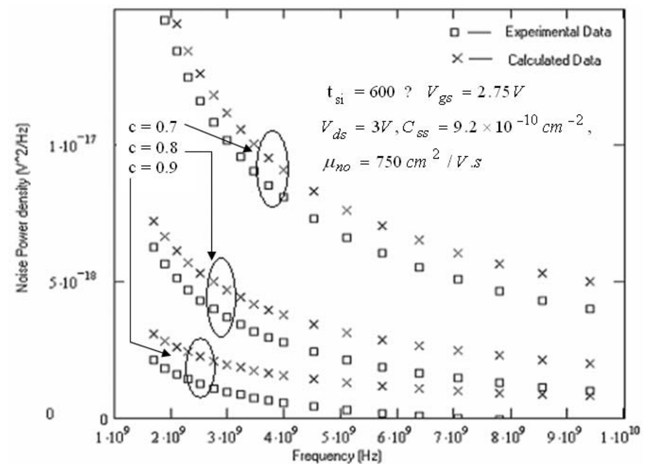

Fig. 3. Noise power spectral density(V^2/Hz) on various values of the exponents c against experimental data. Here, T=179K, N_d=$8\times10^{16}cm^{-3}$, t_{ox}=200Å, Lg=6.0-3.0μm, W=60μm.

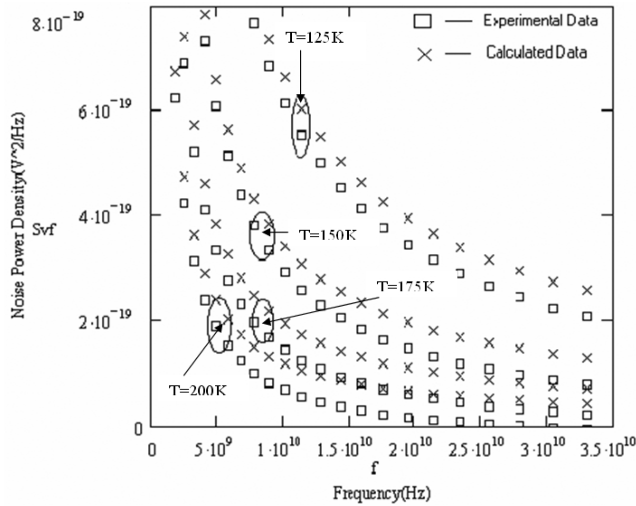

Fig. 4. Noise power spectral density(V^2/Hz) on various values of temperatures increasing downward against experimental data. Here, Lg=0.5μm, W=10μm, t_{si}=600Å, V_{gs}=1.75-3.0V, V_{ds}=3V, c=0.8, t_{ox}=200Å, μ_{no}=750cm²/Vs and C_{ss}=9.2×10^{-10} cm^{-2}.

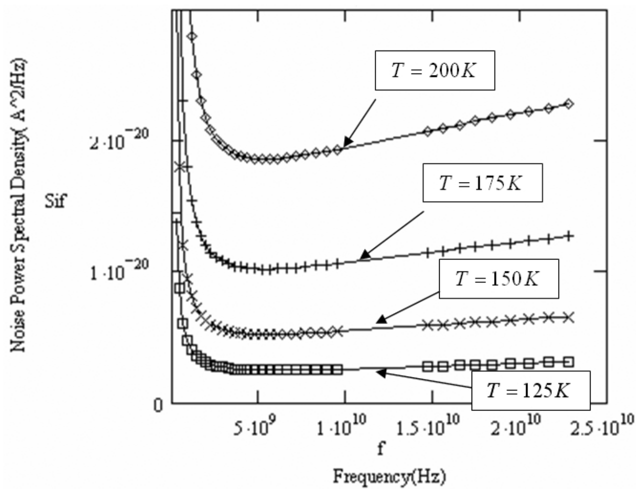

Fig. 5. Noise power spectral density(A^2/Hz) on various values of temperatures increasing upward. Other parameters remain same as above.

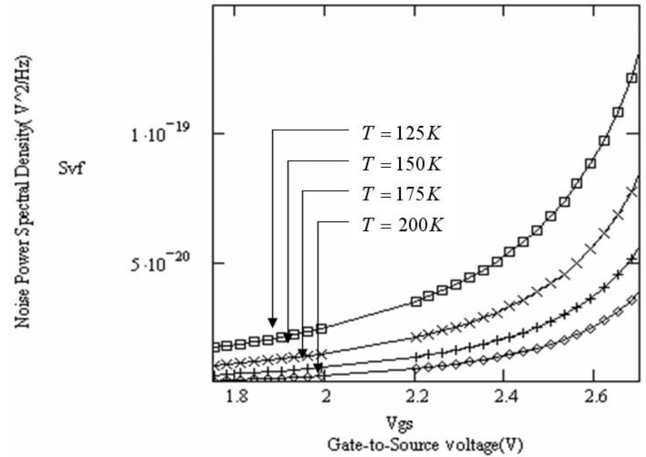

Fig. 6. Calculated Noise power spectral density(V^2/Hz) versus Vgs on various values of temperatures increasing downward. Other parameters remain same as above.

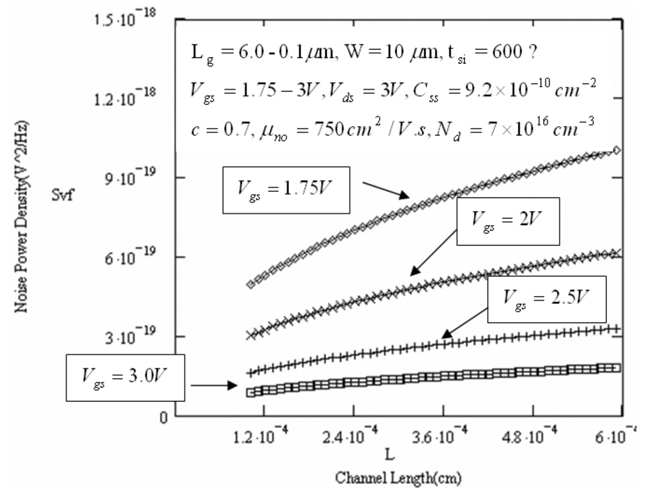

Fig. 7. Calculated Noise power spectral density(V^2/Hz) versus channel length on various values of Vgs increasing downward. T=300 K.

At increasing values of temperature and gate-to-source voltages Noise PSD(V^2/Hz) decreases and NPSD(A^2/Hz) first decreases and then increases at lower value of *c* (shown in the Figure 4 and 5). But as we try to increase the value of exponent *c* Noise PSD becomes constant. Means, when NPSD increases with the increase in Vgs, the flicker noise in the n-channel double-gate SOI MOSFET is due to the mobility fluctuation as the interface trap density varies. On the other hand when we increase the value of the exponent the NPSD attains the constant value which shows *c* the independence from the gate bias voltage and hence the flicker noise here is due to the carrier density fluctuation. In the carrier density fluctuation the interface trap density is usually assumed to be uniform in space and energy.

It shows that it is difficult to say by which means noise is dominated either by carrier-density fluctuation or by mobility-fluctuation due to carrier interactions with lattice fluctuation. We can say that it is consisted of both. As we move from 0.1μn-6.0μn for channel length noise PSD increases with increasing values of gate-to-source voltages(shown in the Figure 6). Because when we increase gate voltage the trap density across the band gets varies. The band bending with increasing gate voltage will

pull down the trap and the trap density fluctuation. Here curve with squares is at lower temperature and curve with diamonds is at higher temperature. The Noise Power Spectral Density versus channel length at various gate to source voltages is shown in Figure 7. It shows that when channel length increases NPSD increases. Because as we increase the channel length, frequency decreases which in turn increases the NPSD.

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