

A Novel Adaptive Biasing Scheme for CMOS Op-Amps

Girish Kurkure and Alope K. Dutta

Abstract—In this paper, we present a new adaptive biasing scheme for CMOS op-amps. The designed circuit has been used in an Operational Transconductance Amplifier (OTA) with ± 1 V power supply, and it has improved the positive and negative slew rates from 2.92 V/msec to 1242 V/msec and from 1.56 V/msec to 133 V/msec respectively, while maintaining all the small-signal performance parameter values the same as that without adaptive biasing (as expected), however, there was a marginal decrease of the dynamic range. The most useful features of the proposed circuit are that it uses a very low number of components (thus not creating severe area penalty) and requires only 25 nW of extra stand-by power.

Index Terms—CMOS, adaptive biasing, differential amplifier, slew rate, low power

I. INTRODUCTION

The speed of high performance mixed signal systems are mainly determined by the settling time of the op-amp [1], which consists of two distinct parts: 1) the slew rate limited period, and 2) the small-signal settling period [2]. Thus, in order to enhance speed, the slew rate of the op-amp should be increased, which in turn requires that the amount of biasing current available to the differential input

stage of the op-amp should be able to charge and discharge the load capacitor within the shortest possible time. Simple techniques of increasing the magnitude of this biasing current are detrimental due consequently to the large power dissipation problem. Reduction of this biasing current, on the other hand, worsens the dynamic characteristics.

A possible solution to optimize these two contradicting circuit performance constraints is to utilize adaptive biasing [3]. In this technique, the concept of an input dependent bias current source is introduced, which results in a low stand-by power dissipation with good dynamic characteristics. Several designs of adaptive biasing circuits have been reported in the literature [4-9], however, almost all of these require additional quiescent current sources, and, thus, result in an increase in the stand-by power dissipation. Only the novel adaptive biasing circuits presented in [7] and [8] do not require any additional quiescent current sources, however, these schemes use too many transistors, which may cause severe area penalty.

Here, we are proposing a new scheme for adaptive biasing, based on the works reported in [7] and [8], keeping three constraints in mind: 1) the circuit should use as few additional components as possible, 2) it should not need any additional quiescent current source, and 3) it should be able to operate under low voltage. Our proposed circuit satisfies all these constraints and requirements to a large extent, and, at the same time, tremendously improves the dynamic response, without affecting the small-signal performance.

II. WORKING PRINCIPLE OF THE PROPOSED CIRCUIT

The schematic of the proposed circuit is shown in Fig.1. Transistors M_1 - M_4 form the core of the circuit. The gates of these transistors are cross-coupled and V_1 and V_2 are the inputs given to these cross-coupled gates. Transistors M_5 and M_6 act as simple current sources, gates of which are connected to the drains of M_2 and M_4 respectively. Transistor M_7 provides a low impedance load to M_5 / M_6 and samples the current flowing through these transistors, while transistor M_8 mirrors the current flowing through M_7 . In order to get sufficient current amplification, an additional current mirror M_9 - M_{10} may be used for cases, where the requirements dictate its use.

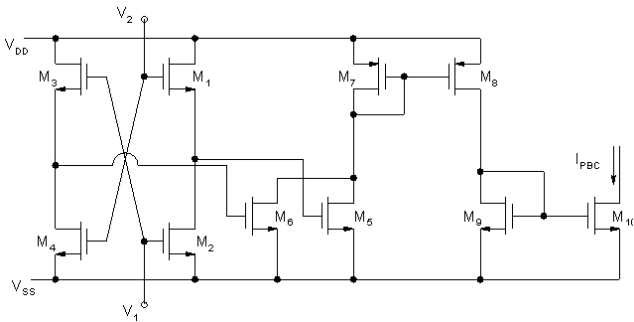


Fig. 1. The schematic of the proposed adaptive biasing circuit.

M_1 and M_4 are chosen to have the same aspect ratio (i.e., the W/L ratio, where W and L are the width and length of the MOSFETs respectively). Thus, when the voltages at the gates of M_1 and M_2 are equal, the gate-to-source voltage of M_2 will be higher as compared to that of M_1 . However, since both these transistors are connected in series, hence, the current flowing through both of them must be the same. This is possible only if M_2 goes into the triode mode of the weak-inversion region. Thus, in this case, the voltage at the gate of M_5 will be very close to the negative power supply voltage V_{SS} . The same statement holds true also for the case of M_3 - M_4 combination. Now, even when the voltages at the gates of M_1 and M_3 are less than the voltages at the gates of M_2 and M_4 respectively, even then M_2 and M_4 will remain in the triode region of weak inversion. In this case also, the gate voltages of M_5 and M_6 [$V_G(M_5)$ and $V_G(M_6)$ respectively] will be very close to V_{SS} . Thus, $V_G(M_5) \approx V_{SS}$ for $V_2 \leq V_1$.

As we start increasing the voltage at the gate of M_1 (or M_3) as compared to that of M_2 (or M_4), then M_2 (or M_4) would come out of the triode region, and both the upper as well as the lower transistor in each branch would now be operating in the saturation mode of the weak- or strong-inversion region, depending upon the magnitude of the input voltage. Thus, in this case from $I_{D1} = I_{D2}$, where I_{D1} and I_{D2} are the drain currents of M_1 and M_2 respectively, we get $V_{GS1} = V_{GS2}$. Thus, for this case, $V_G(M_5) = [(V_2 - V_1) + V_{SS}]$ for $V_2 \geq V_1$. Similar conditions for $V_G(M_6)$ can be given by $\approx V_{SS}$ for $V_1 \leq V_2$, and $[(V_1 - V_2) + V_{SS}]$ for $V_1 \geq V_2$. M_5 remains in the subthreshold region of operation as long as $(V_2 - V_1) \leq V_{TN}$, where V_{TN} is the threshold voltage of the NMOS devices. Similarly, M_6 remains in the subthreshold region of operation as long as $(V_1 - V_2) \leq V_{TN}$.

When the gate voltages of M_5 and/or M_6 are close to V_{SS} , both remain in the off state, since their gate-to-source voltages are not sufficient for them to conduct. However, when the gate voltages of M_5 or M_6 vary proportionately to the difference between the two input signals, then the current flow through these devices would also vary with the differential input voltage. Using current samplers and mirrors, these currents can be sensed and amplified subsequently and can be used to bias any differential amplifier (DA) or operational transconductance amplifier (OTA) adaptively, where this additional bias current would be proportional to the differential input signal. Thus, the drain current for M_7 can be given by $I_D(M_7) = I_D(M_6)$ (for $V_1 > V_2$), $I_D(M_5)$ (for $V_1 < V_2$), and ≈ 0 (for $V_1 \approx V_2$). Here, M_5 and M_6 are assumed to be identical. If M_7 and M_8 have an aspect ratio of $1:A_1$, then $I_D(M_8) = I_D(M_7) = A_1 I_D(M_7)$. Similarly, if M_9 and M_{10} have an aspect ratio of $1:A_2$, then $I_D(M_{10}) = A_2 I_D(M_9) = I_{PBC}$, where I_{PBC} is the bias current produced by the proposed biasing circuit. By properly choosing A_1 and A_2 , this additional bias current, which is proportional to the differential input signal, can be made large, thus improving the slew rate tremendously.

III. SIMULATION RESULTS

The TANNER EDA tool [10] has been used for all the simulations with $0.5 \mu\text{m}$ technology file, supported by the BSIM3v3 model [11]. The supply voltages (V_{DD} and V_{SS})

used are ± 1 V. Note that depending on the relative magnitudes of V_1 and V_2 , the devices used in the adaptive biasing block may either be in the weak- or strong-inversion region. When V_1 (or V_2) is varied from $+1$ V to -1 V, holding V_2 (or V_1) to zero, the gate-to-source voltages of M_5 and M_6 would vary as described in Section II. Figure 2 shows the variation of the output bias current I_{PBC} of the adaptive biasing block, proposed in this work here, as a function of the differential input voltage within a range of ± 1 V.

Two important features can be observed from Fig.2. One is the existence of something like a dead band, which is roughly between ± 0.5 V, which is common to all the adaptive biasing blocks proposed earlier. The additional bias current available in this band is not much, but not zero either, so a finite improvement in the dynamic response can be expected even here. The other feature is that as the differential input voltage approaches its maximum value of ± 1 V, the additional bias current provided by this block is more than $350 \mu\text{A}$, which is indeed a substantial increase, and should improve the dynamic response tremendously.

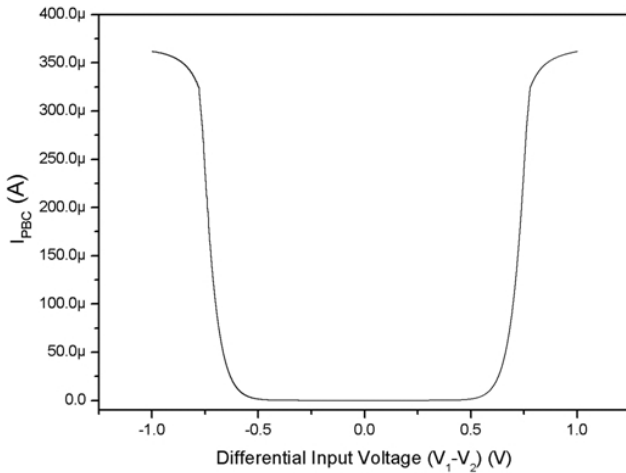


Fig. 2. The output current (I_{PBC}) of the proposed adaptive biasing block as a function of the differential input voltage ($V_1 - V_2$) within a range of ± 1 V.

In order to test the efficacy of the proposed circuit, we have considered a conventional OTA [12], with local common mode feedback resistances R_1 and R_2 and without any adaptive biasing. Figure 3 shows the schematic of the OTA with the proposed adaptive biasing block included, however, the output stage M_9 - M_{10} of the proposed block is not used here, instead, the aspect ratio of M_7 - M_8 is suitably adjusted. The OTA of Fig.3 is biased with a constant

current of $5 \mu\text{A}$, which is controlled by V_{BIAS} , in quiescent state. In the stand-by mode, the proposed adaptive biasing circuit provides extremely small additional current as compared to the current provided by the constant current source. Thus, the transconductance and the output resistance of the transistors used in the OTA remain unaffected, and, hence, the small-signal performance parameters show absolutely no change, as expected.

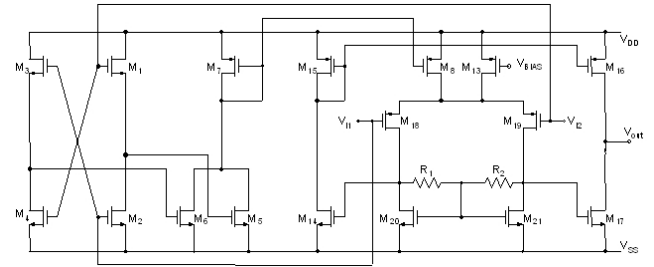


Fig. 3. The schematic of the OTA [18] with the adaptive biasing circuit, proposed in this work, included.

In particular, the small-signal low-frequency voltage gain and the gain-bandwidth product remain pegged at 28.2 dB and 18.23 MHz, both without and with the proposed adaptive biasing circuit. Similarly, the positive and negative power supply rejection ratios PSRR^+ and PSRR^- remain at 28.83 dB and 78.34 dB respectively, both without and with the proposed circuit. The same behavior is exhibited by the noise spectral density at 100 kHz, which remains constant at $2.25 \mu\text{V}/\sqrt{\text{Hz}}$ for both the circuits. However, there is a small decrease of the output range, i.e., the OTA without adaptive biasing had a swing of $+913$ mV to -915 mV, whereas the swing for the OTA with the proposed circuit is from $+907$ mV to -902 mV. This small reduction in the output range is due to the nonlinearity introduced by the adaptive biasing block.

In order to obtain the transient response of the OTA, a square wave of 250 kHz frequency with an amplitude of ± 1 V is applied at the input V_{in} while keeping the other input grounded. A load capacitance of 1 pF is used for obtaining the transient response and the slew rate characteristics. It was observed that the transient performance of the adaptively biased OTA is far superior than that of the OTA without any adaptive biasing. The settling time of the output of the OTA decreased from 684 ns to only 1.61 ns for a -1 V to $+1$ V transition at the input, and from 1.28 μs to 15 ns for a $+1$ V to -1 V input

transition. The positive slew rate has thus increased from 2.92 V/ μ s to 1242 V/ μ s, and the negative slew rate from 1.56 V/ μ s to 133 V/ μ s.

The most interesting feature of this adaptive biasing circuit is that it requires negligible amount of additional quiescent power, which is approximately only 250 nW. Moreover, the additional transistor count is also very low, resulting in lesser area overhead requirements and lesser amount of noise introduction. Of course, the improvement in the dynamic response will be less dramatic for an input pulse having lesser differential amplitude. Incidentally, the additional circuit has no effect on the total harmonic distortion as well, which remains the same for the OTA both without and with adaptive biasing.

IV. SUMMARY AND CONCLUSIONS

In this paper, we have presented a novel adaptive biasing scheme for differential amplifiers. In order to test the efficacy of the designed circuit, it was employed on an OTA, and both large- and small-signal behavior of the OTA were simulated using Tanner-Spice with BSIM 3v3 technology file. It is observed that the addition of this adaptive biasing block improves the dynamic performance, in particular, the slew rates tremendously, without adversely affecting other small-signal parameters. Also, it does not require any quiescent current source, needs only 250 nW of additional quiescent power, and has a very low additional transistor count, thus not amounting to a severe area penalty. The designed circuit has a great prospect of becoming highly useful for low power circuits to improve their dynamic response.

REFERENCES

1. J. M. Shin and K. S. Yoon, "Design of a Programmable Slew Rate Op-Amp," *Proc. of the 37th Midwest Symp. Circ. & Syst.*, LA, vol. 1, pp. 142-146, August 1995.
2. B.W. Lee and B.J. Sheu, "A High Slew Rate CMOS Amplifier for Analog Signal Processing," *IEEE J. Solid-St. Circ.*, vol. SC-25, no. 3, pp. 885-889, June 1990.
3. M. G. Degrauwe, J. Rijmenants, E.A. Vittoz, and H. J. DeMan, "Adaptive Biasing CMOS Amplifiers," *IEEE J. Solid-St. Circ.*, vol. SC-17, no. 3, pp. 522-528, June 1982.
4. B. J. Blalock and P. E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology," *Proc. IEEE Int. Symp. Circ. & Syst.*, Seattle, pp. 1972-1975, May 1995.
5. S. Baswa, A. J. Lopez-Martin, R. G. Carvajal, and J. Ramirez-Angulo, "Low-Voltage Power Efficient Adaptive Biasing for CMOS Amplifiers and Buffers," *Electron. Lett.*, vol. 40, no. 4, pp. 217-219, February 2004.
6. G. Ferri, "Low-Voltage Low-Power Adaptive Biased High-Efficiency Integrated Amplifiers," *8th IEEE Int. Conf. Elect., Circ., & Syst. (ICECS)*, vol. 3, pp. 1529-1532, 2001.
7. G. C. Cardarilli and G. Ferri, "CMOS Adaptive Biasing Circuits for Low-Power Applications," *Proc. 21st Int. Conf. Microelect.*, vol. 2, pp. 14-17 and 747-750, September 1997.
8. G. C. Cardarilli and G. Ferri, "Dynamic Biased Topologies for Low Power Bipolar Application," *Euro. Conf. Circ. Theory & Des. (ECCTD)*, Budapest, pp. 1438-1441, August-September 1997.
9. G. Giustolisi, G. Palmisano, and T. Segreto, "1.2 V CMOS Op-Amp with a Dynamically Biased Output Stage," *IEEE J. Solid-St. Circ.*, vol. SC-35, no. 4, pp. 632-636, April 2000.
10. "T-Spice™ User Guide and Reference," Tanner EDA, Pasadena, 1998.
11. W. Liu, "MOSFET Models for SPICE Simulation, Including BSIM3v3 and BSIM4," Wiley, Britain, 2001.
12. J. Ramirez-Angulo and M. Holmes, "Simple Technique Using Local CMFB to Enhance Slew Rate and Bandwidth of One-Stage CMOS Op-Amps," *Electron. Lett.*, vol. 38, no. 23, pp. 1409-1411, November 2002.



Girish M. Kurkure He received the B.E. degree in Electronics and Telecommunication Engineering from Govt. Engg. College, Ujjain, India, in 1999, and M.Tech degree in Electrical Engineering from Indian Institute of Technology, Kanpur, India, in 2004. From 2000-2002, he taught at the undergraduate level at the Bansal Institute of Science and Technology, Bhopal, India. Presently, he is an Executive Engineer in the Information Technology and Innovation Center at Reliance Infocomm Pvt. Ltd. His research interests are low-voltage low-power analog circuit design and interference cancellation in wireless communication.



Alope Kumar Dutta He was born in Calcutta, India, in 1960. He received the B.E. degree in Electrical Engineering from Jadavpur University, Calcutta, India, in 1982, and the M.S. and Ph.D. degrees In Electrical Engineering from Louisiana State University, Baton Rouge, La, USA, in 1985 and 1989, respectively. In 1990, he joined the Indian Institute of Technology, Kanpur, India, as an Assistant Professor, where he is currently a full Professor. His current research interests are focused in submicron MOSFET modeling, mixed-signal low-power low-voltage VLSI, and RF circuits. He is a member of Eta Kappa Nu and Phi Kappa Phi.