

A High-Density 64k-Bit One-Time Programmable ROM Array with 3-Transistor Cell Standard CMOS Gate-Oxide Antifuse

Hyouk-Kyu Cha, Jinbong Kim*, and Kwyro Lee

Abstract—A high-density 3-transistor cell one-time programmable (OTP) ROM array using standard CMOS Gate-Oxide antifuse (AF) is proposed, fabricated, and characterized with $0.18\mu\text{m}$ CMOS process. The proposed non-volatile high-density OTP ROM is composed of an array of 3-T OTP cells with the 3-T consisting of an nMOS AF, a high voltage (HV) blocking transistor, and a cell access transistor, all compatible with standard CMOS technology.

I. INTRODUCTION

The CMOS OTP ROM, among various memory types, is one of the cheapest nonvolatile memories in comparison to flash memories because of its additional processes [1-3]. There are many types of OTP, and most of them are based on either fusing or anti-fusing. These types include poly fusing using laser instrument and joule heating [4,5], and oxide-nitride-oxide (ONO) antifusing [6]. One of the most promising choice as an antifuse element with standard CMOS technology is the gate oxide. Until recently, gate oxide breakdown voltage has been much higher than that of the power supply. However, due to the continued scaling of gate oxide which is much faster than the power supply voltage scaling, we are now able to consider antifuse based on a very thin gate oxide [7]. In this paper, we report a high-density OTP ROM array using 3-T OTP cell based on thin gate oxide AF which is fully compatible with standard CMOS process technology.

Manuscript received May 30, 2004; revised June 19, 2004.

Dept. of EECS, KAIST also with MICROS Research Center, Daejeon 305-701

*System IC LDI team1, Hynix Semiconductor Inc., Cheongju 361-725

PACS numbers : 85.30.Mn, 84.30.Bv

Keywords : CMOS antifuse, CMOS OTP ROM

TEL: +82-42-869-8033 FAX +82-42-869-8590

E-mail : hkcha98@dimple.kaist.ac.kr

II. CMOS antifuse

Fig. 1 shows the cross-sectional view of nMOS AF in programming mode (PGM) where high voltage of V_{PP} whose value is much higher than that of the power supply V_{DD} is applied to the gate of the AF. The channel is inverted and the source/drain edge regions below the gate are accumulated, which favor higher electric field in edges and channel regions.

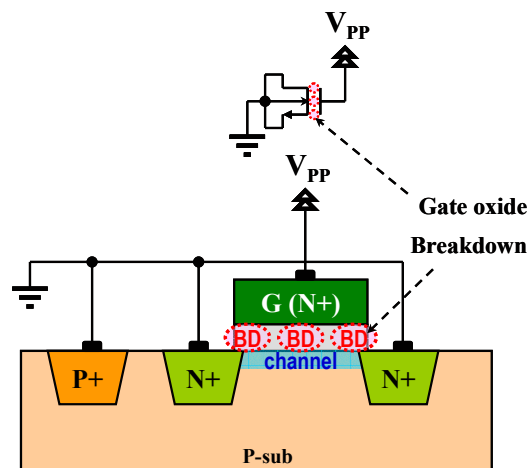


Fig. 1. nMOS AF structure

Before the programming high-voltage is applied to the gate, that is, before the breakdown, the gate current characteristics show tunneling with large pre-breakdown resistance of R_{OFF} , which is higher than $1\text{G}\Omega$ at $V_{PP} = 2.0\text{V}$. However, the gate oxide is broken down permanently when V_{PP} is higher than 5.8V for $0.18\mu\text{m}$ CMOS process (gate oxide thickness of $T_{OX} = 37\text{\AA}$). During the breakdown of the AF, the increasing current supply reduces the value of R_{ON} (post-breakdown resistance) [8]. Fig. 2 shows the cumulative distributions of R_{ON} for each 200 nMOS samples after oxide breakdown with different current compliances ($CC = 1\text{mA}$, 0.3mA , and 0.1mA), 100ms duration, and the

applied V_{PP} of 6.5V. After AFs are broken-down, R_{ON} values are measured at the V_{PP} of 1.5V using Ohm's law. These similar phenomena occur in pMOS AF as well.

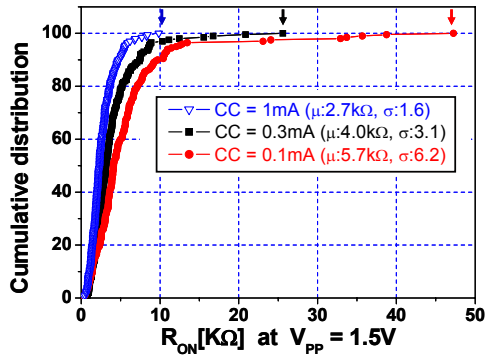


Fig. 2. The measured R_{ON} distributions for each 200 samples with three different current compliances (1mA, 0.3mA, and 0.1mA)

III. High-Density CMOS OTP ROM

Fig. 3 shows the basic 3-transistor OTP ROM cell array utilizing the CMOS AF as the storage element. The 3-T OTP cell is composed of an nMOS AF (AF), a HV blocking nMOS (BM), and a cell access transistor (AT). As it can be seen in the figure, in the PGM mode, HV is applied to the tied gates of all AF's (V_{PP} node) and only one AF that is programmed (that breaks down) is the one that is selected by the corresponding word-line (WL) and bit-line (BL). In the reading mode (READ), V_{DD} is instead applied to the V_{PP} node. In the programmed cell, the current flows through the AF to BL, which can be detected by a current sense amplifier located in BL while very small tunneling current ($<100\text{pA}$) flows through the non-programmed antifuse cell [9].

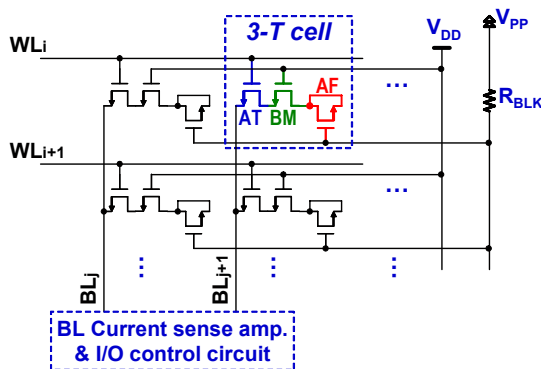


Fig. 3. The basic 3-transistor OTP ROM cell array utilizing the CMOS AF

Using the basic 3-transistor OTP ROM cell, a high-density OTP ROM array is implemented, as shown in Fig. 4.

Fig. 4(b), (c), (d), and (e) show various operation conditions during programming mode in selected/non-selected cells. In the selected cell shown in Fig. 4(b), immediately after AF breakdown, HV would be applied to the drain-substrate junction of the BM in case of small R_{ON} . In order to prevent this situation, a blocking resistor (R_{BLK}) is inserted in series with HV supply node, which also helps in keeping constant current level for uniform AF rupturing at the same time. The non-selected cell with already broken AF is shown in Fig. 4(d) where HV is now applied directly to the drain-substrate junction of BM. This HV does not affect the blocking nMOS in a destructive way since AT is now in OFF-state. A small amount of gate induced drain leakage (GIDL) current of BM flows through drain-to-substrate junction, which is non-destructive during long-programming duration.

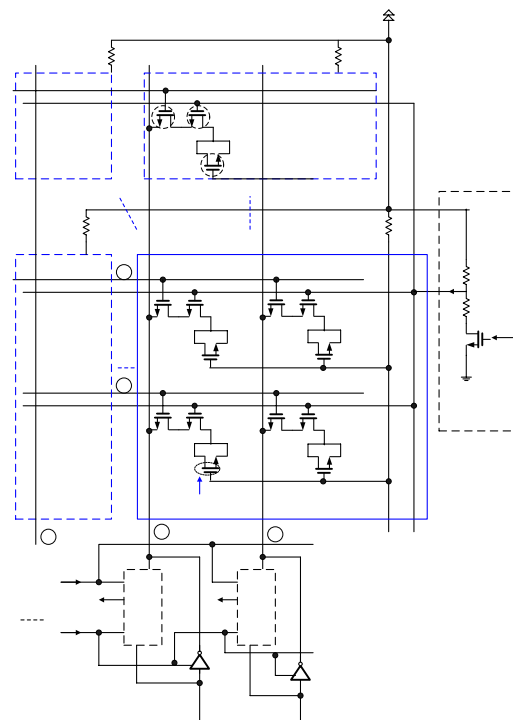


Fig. 4. The structure of high-density OTP ROM (a) 3-T OTP cell (b) selected cell, (c) non-selected cell, (d) non-selected cell with already broken AF, (e) non-selected cell, and (f) global V_{G-BM} generation circuit

Figs. 4(c) and (e) show the case of non-selected cell with unbroken AF where no disturbance problems have been found. The tied drain/source node voltage of antifuse is high that the gate oxide of antifuse does not rupture during programming. The high-voltage is divided by the ratio of two currents – the tunneling

current of unbroken AF and the GIDL current of BM. The measured results show that less than 10pA of current flows when the high-voltage of 6.5V is applied to the AF node and that the AF breakdown voltage is at least 10V.

To implement the high-density structure shown in Fig.4, issues such as smaller area consumption and reliable operation has to be considered. The CMOS antifuse OTP ROM uses a high-voltage node to program the storage cell, and the programming time, which is the time-to-breakdown of MOSFET, greatly depends on the programming high-voltage. The reliable structure for high-voltage and long programming duration is therefore necessary.

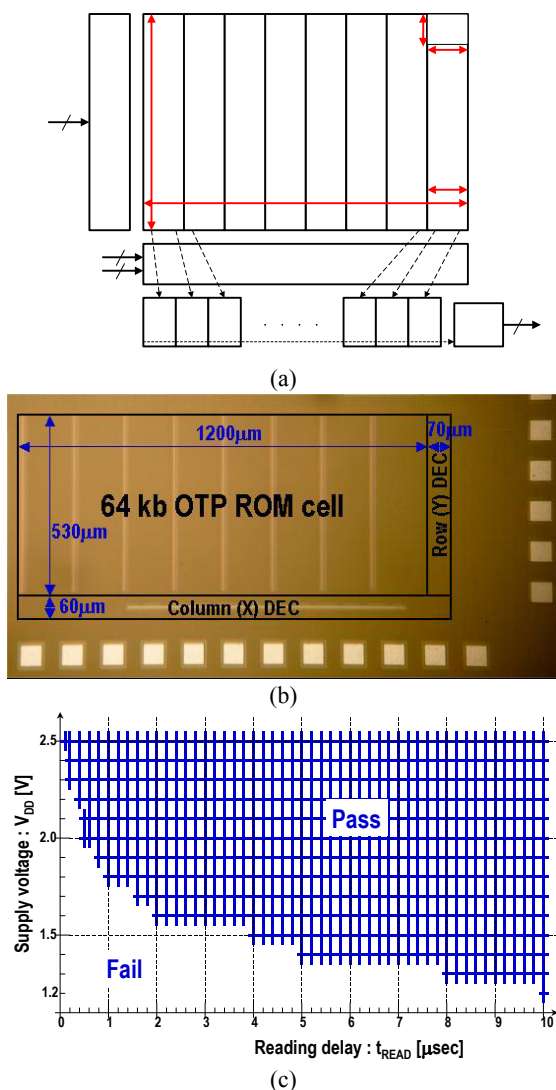


Fig. 5. (a) The structure of 64-kbit OTP ROM, (b) the implemented chip microphotograph with Anam 0.18 μ m process, and (c) measurement results-Shmoo plot during reading mode operation

From these considerations, we have designed the high-

density 64-kbit OTP ROM array, its structure shown in Fig. 5(a), fabricated with Anam 0.18 μ m CMOS process and measured with a logic analysis system and a pattern generator. The 64-kb OTP ROM array consists of address decoders (WL and BL) and input/output peripherals including the current sense amplifiers. Eight 8-kb cells with 128 unit blocks consist the whole 64-kb cell array, while the unit block is composed of 64-bit 3-T cells and a blocking resistor of R_{BLK} .

These cells are accessed by 256 of word lines and bit lines, respectively, decoded from 16-bit address signals which are inputted from external pins. Its implemented chip microphotograph and measured result, which is the Shmoo plot showing the supply voltage vs. reading delay during the reading mode, are shown in Fig. 5(b) and (c). The unit 3-T cell area is about 10 μ m², while its overall area is below 1.3 \times 0.6mm².

IV. CONCLUSION

In this paper, we have proposed the non-volatile high-density OTP ROM based on 3-T cell OTP ROM array, which is composed of an nMOS AF, BM and AT, all compatible with standard CMOS technology. From the measurement of 64-kbit OTP ROM, we are able to conclude that the proposed structure can be a viable technology for modern digital as well as analog circuits.

REFERENCES

- [1] B.J. Shin, K.K. Park, and S.I. Yang, J. Korean Phys. Soc. 41, 801 (2002)
- [2] B. Kim, S.E. Lee, and K.Y. Seo, J. Korean Phys. Soc. 40, 642 (2002)
- [3] I.H. Cho, B.G. Park, J.D. Lee, and J.H. Lee, J. Korean Phys. Soc. 42, 233 (2003)
- [4] C.Y. Lu, J.D. Chlipala, and L. M. Scarfone, *IEEE Transaction on Electron Devices* 36, 1056 (1989)
- [5] O.Kim, C.J.Oh and K.S.Kim, *Electronics Letters*, 34, 355 (1998)
- [6] J.K. Wee, J.H. Kook, S.H. Hong, and J.H. Ahn, J. Semicon. Tech. Sci, 1, 216 (2001)
- [7] J. Kim, K. Lee, *Symp. On VLSI Circuits 2003*, 223 (2003)
- [8] B.P. Linder, et al, *SOVT 2000*, 214, 2000
- [9] J. Kim, K. Lee, *IEEE Elec. Dev. Lett.* 24, 589 (2003)



Hyouk-Kyu Cha was born in Seoul, Republic of Korea, in 1979. He received the B.S. degree in Electrical Engineering and Computer Science (EECS) from Korea Advanced Institute of Science and Technology (KAIST), in Daejon, Korea, in 2003.

He is currently pursuing the M.S. degree in EECS from KAIST. His current research activities include CMOS One-Time-Programmable (OTP) ROM design and its applications.



Jinbong Kim was born in Changwon, Republic of Korea, in 1971. He received the B.S., M.S., and Ph.D degrees in Electrical Engineering and Computer Science (EECS) from Korea Advanced Institute of Science and Technology (KAIST), Daejon, Korea,

in 1997, 1999, and 2004, respectively. He currently works at Hynix Semiconductor Inc., Cheongju, Korea. His current research interests are in CMOS non-volatile memories and Microcontroller units.



Kwyro Lee received the B.S. degree in Electronics Engineering from Seoul National University in 1976 and the M.S. and Ph.D degrees from the University of Minnesota, Minneapolis in 1979 and 1983, respectively, where he did many

pioneering works for modeling Heterojunction Field Effect Transistor. After graduation, he worked as an Engineering General Manager in Goldstar Semiconductor Inc. Korea, from 1983 to 1986, responsible for development of first polysilicon CMOS products in Korea. He joined KAIST in 1987 in the department of Electrical Engineering and Computer Science, where he is now a Professor. His research interests are focused on RF device, circuit and ploylithic integration of heterogeneous system on a single chip. He led the development of AIM-Spice and is the principal author of the book titled, "Semiconductor Device Modeling for VLSI", 1993, Prentice Hall. He is a Senior Member of IEEE and a Life Member of IEEK. He served as the Chairman of IEEE Korea Electron Device Chapter and is currently serving as the elected member of IEEE EDS AdCom. He has also been working as the Director of MICROS (Micro Information and Communication Remote-object Oriented Systems) Research Center since 1997.