

Theoretical and Experimental Analysis of Back-Gated SOI MOSFETs and Back-Floating NVRAMs

Uygar Avci, Arvind Kumar*, and Sandip Tiwari*

Abstract—Back-gated silicon-on-insulator MOSFET - a threshold-voltage adjustable device-employs a constant back-gate potential to terminate source-drain electric fields and to provide carrier confinement in the channel. This suppresses short-channel effects of nano-scale and of high drain biases, while allowing a means to threshold voltage control. We report here a theoretical analysis of this geometry to identify its natural length scales, and correlate the theoretical results with experimental device measurements. We also analyze experimental electrical characteristics for misaligned back-gate geometries to evaluate the influence on transport behavior from the device electrostatics due to the structure and position of the back-gate. The back-gate structure also operates as a floating-gate non-volatile memory (NVRAM) when the back-gate is floating. We summarize experimental and theoretical results that show the nano-scale scaling advantages of this structure over the traditional front floating-gate NVRAM.

I. INTRODUCTION

Double-gate MOSFET has been a subject of large interest for scalable and nano-scale MOSFET [1,2] for a considerable period of time. However, predominant interest in this structure is related to achieving the structure in

thin single-crystal silicon where transport is controlled by symmetric gates with symmetric dielectrics. One reason for this is the ease with which fin-based FETs can be fabricated as well as the focus on high performance and high current drive that naturally gravitates to thinnest oxides and shortest gate lengths. Viewed from power and device density perspective, optimization of power and speed via a second gate that controls the threshold voltage and the minimization of the space penalty that this second gate brings are very important goals. The back-gate structure achieves this by providing an asymmetric configuration in oxide thickness and an independent control to the second gate in circuits without a significant area penalty (**Fig. 1a**). By varying the back-gate potential, this structure can operate as a threshold-voltage adjustable device. This is essential for power-adaptive high-density system designs.

Physical models have been developed to understand short-channel effects of fully-depleted SOI transistors [3-5]. Yan et al. [3] proposed the use of a parameter called natural length scale that allows comparison of scalability of different MOSFET structures and used this technique to investigate the scalability of single-gate SOI MOSFET and double-gate MOSFET. We extend this technique to the back-plane CMOS geometry and use experimental [6] and simulation results to correlate. While an ideal back- and front-gated back-plane transistor will have self-aligned gates to allow minimization of capacitive effects, and such structures are being explored and evaluated, here we focus on structures where the back-gate can be misaligned from the front-gate. So, the back-gate can be shifted either towards the source or the drain, with interesting consequences for

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School of Applied and Engineering Physics, *School of Electrical
and Computer Engineering Cornell University, Ithaca, NY 14853

the transport and the gate control due to electrostatic effect from the geometrical structure. These are evaluated to emphasize the importance and interesting consequences for devices useful for a range of applications.

The back-plane structure can also operate as a non-volatile memory when the back-gate is floating. Such a structure is identical in nearly all respects to the logic transistor structure. But, this back-floating NVRAM structure decouples the read operation from write operation allowing the front-gate oxide to be scaled consistent with CMOS scaling while protecting the charge leakage at the bottom interface for non-volatile operation. Here, we show the behavior of the back-gate structure as a back-floating NVRAM and demonstrate the speed advantages due to efficient hot electron injection that the new geometry provides.

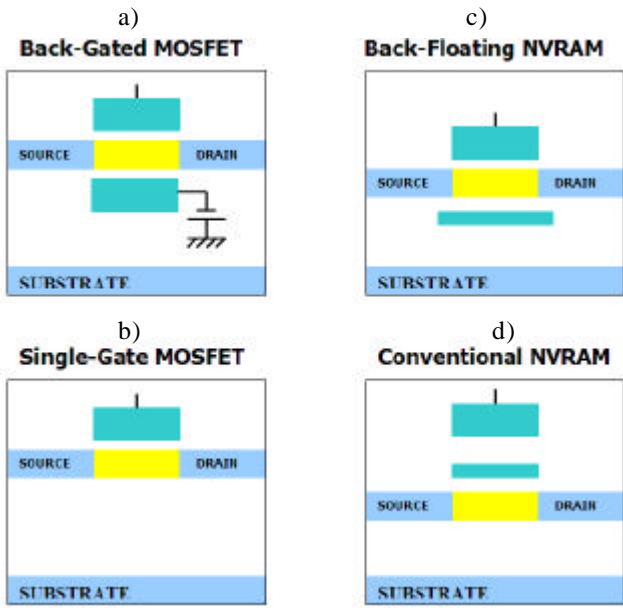


Fig.1. shows the transistors: a) back-gated SOI MOSFET, b) the conventional single-gate SOI MOSFET, and the non-volatile memories: c) back-floating gate NVRAM, d) conventional floating-gate NVRAM.

II. BACK-GATED SOI MOSFET

1. Scaling Theory

An approach to analyzing the complex thin-silicon based structures, such as of SOI MOSFET [3] and the double-gate MOSFET [5] has been to analyze the

electrostatics through parameterization of the Poisson's equation [7]. These geometries have boundary conditions that may be symmetric, e.g., the classical double-gate, or single-gate, e.g., the SOI. We employ this approach and extend it to the asymmetric back-gate in this approach.

Before strong-inversion, with the electron charge density low, the two-dimensional potential distribution is described by:

$$\frac{d^2\Phi(x, y)}{dx^2} + \frac{d^2\Phi(x, y)}{dy^2} \cong \frac{qN_A}{\epsilon_{Si}} \quad (1)$$

$$\Phi(x, y) \approx c_0(x) + c_1(x)y + c_2(x)y^2 \quad (2)$$

where $\Phi(x, y)$ is the potential, x is the lateral source-to-drain direction, y is the cross-sectional front-channel-to-back-channel direction, q is the electronic charge, N_A is the acceptor density and ϵ_{Si} is the dielectric constant of silicon. The solution to the potential is a polynomial of power 2 because of constant doping.

The boundary conditions are:

1) The potential at the front-interface:

$$\Phi(x, 0) = \Phi_F(x) = c_0(x), \quad (3)$$

2) from the electric field at the front-interface:

$$\left. \frac{d\Phi(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{Ox}}{\epsilon_{Si}} \frac{\Phi_F(x) - V_{Fgs}}{t_{Fox}} = c_1(x), \quad (4)$$

3) the potential at the bottom interface:

$$\Phi(x, t_{Si}) = \Phi_B(x) = c_0(x) + c_1(x)t_{Si} + c_2(x)t_{Si}^2, \quad (5)$$

4) and from the electric field at the bottom-interface:

$$\left. \frac{d\Phi(x, y)}{dy} \right|_{y=t_{Si}} = \frac{\epsilon_{Ox}}{\epsilon_{Si}} \frac{V_{Bgs} - \Phi_B(x)}{t_{Box}} = c_1(x) + 2t_{Si}c_2(x) \quad (6)$$

Using these boundary conditions, $F(x,y)$ can be written as a function of $F_F(x)$ and y , where $F_F(x)$ is the potential at the front-channel. Substituting this function in (1) and defining a dummy potential $F'(x)$, which differs from the $F_F(x)$ by only a constant:

$$\Phi'(x) = \Phi_F(x) + \frac{qN_A}{e_{Si}} I_{BG}^2 - \frac{I_F^2}{I_F^2 + I_B^2 + t_{Si}^2} V_{Bgs} - \frac{I_B^2 + t_{Si}^2}{I_F^2 + I_B^2 + t_{Si}^2} V_{Fgs} \quad (7)$$

We can now write the Poisson's equation as:

$$\frac{d^2 \Phi'(x)}{dx^2} - \frac{\Phi'(x)}{I_{BG}^2} = 0 \quad (8)$$

where:

$$I_F^2 = \frac{e_{Si}}{e_{Ox}} t_{Fox} t_{Si} \quad I_B^2 = \frac{e_{Si}}{e_{Ox}} t_{Box} t_{Si}$$

and

$$I_{BG}^2 = I_F^2 \frac{2I_B^2 + t_{Si}^2}{2I_B^2 + 2t_{Si}^2 + 2I_F^2} \quad (9)$$

The one-dimensional equation (8), where the '?'s have been introduced as parameters, can be solved using the source and drain boundary conditions:

$$\Phi'(0) = \Phi_S \quad \Phi'(L_G) = \Phi_D = \Phi_S + V_{DS} \quad (10)$$

The solution is:

$$\Phi'(x) = \frac{\Phi_S \sinh((L_G - x)/I_{BG}) + (\Phi_S + V_{DS}) \sinh(x/I_{BG})}{\sinh(L_G/I_{BG})} \quad (11)$$

Equation (11) provides the front-interface potential (with a constant difference) for the back-gated SOI MOSFET prior to the strong inversion. Since the conduction is barrier-modulated in this state, the peak of the barrier can represent the level of conduction. By

equating the differential of the potential to zero, the point where the potential has a peak, and the minimum of dummy potential value, can be found as:

$$x_{\min} \cong \frac{L_G}{2} - \frac{I_{BG}}{2} \ln \left(1 + \frac{V_{DS}}{\Phi_S} \right) \quad (12)$$

$$\Phi'_{\min} \cong 2e^{\frac{-L_G}{2I_{BG}}} \sqrt{\Phi_S (\Phi_S + V_{DS})} \quad (13)$$

Here we assumed that $e^{(-L_G/2I_{BG})} \ll 1$. Inserting (13) in (7), F_{\min} is found to be:

$$\Phi_{F_{\min}} = 2e^{\frac{-L_G}{2I_{BG}}} \sqrt{\Phi_S (\Phi_S + V_{DS})} - \frac{qN_A}{e_{Si}} I_{BG}^2 + \frac{I_F^2}{I_F^2 + I_B^2 + t_{Si}^2} V_{Bgs} + \frac{I_B^2 + t_{Si}^2}{I_F^2 + I_B^2 + t_{Si}^2} V_{Fgs} \quad (14)$$

This potential can be used to evaluate the inverse sub-threshold slope:

$$S = \ln(10) \frac{kT}{q} \left(\frac{\partial \Phi_{F_{\min}}}{\partial V_{Fgs}} \right)^{-1} = S_{Ideal} \left[1 - \frac{I_F^2}{I_F^2 + I_B^2 + t_{Si}^2} \right]^{-1} \left[1 - \frac{2\Phi_S + V_{DS}}{\sqrt{\Phi_S (\Phi_S + V_{DS})}} e^{\frac{-L_G}{2I_{BG}}} \right]^{-1} \quad (15)$$

Similarly, the drain-induced barrier-lowering (DIBL) is the difference between front gate voltages that provide the same surface potential for two different drain biases:

$$\Delta V_T(DIBL) \cong \left[1 - \frac{I_F^2}{I_F^2 + I_B^2 + t_{Si}^2} \right]^{-1} 2e^{\frac{-L_G}{2I_{BG}}} \sqrt{\Phi_S} (\sqrt{\Phi_S + V_{DS}} - \sqrt{\Phi_S}) \quad (16)$$

The parameter λ_{BG} , in these equations represent a natural length scale that defines the dimension where short channel consequences become more pronounced. Note, e.g., that smaller natural length scale (λ_{BG}) means device is more scalable since it gives more ideal sub-threshold-slope in (15) and lower DIBL in (16). It can be observed in (9) by substituting λ_B with infinity (thick back-gate oxide) that natural length scale for single-gate SOI device is simply λ_F as shown in [3] which is always larger than λ_{BG} , since the second-term of λ_{BG} is smaller than unity. Because of the capacitive coupling of back-gate to front-gate, the inverse sub-threshold slope of back-gated device is larger than the one for single-gate

SOI for long-channel devices which is dictated by the second term of (15). However, as the devices scale (decreasing L_G), the exponential terms in both inverse sub-threshold slope and DIBL becomes more significant and the back-gated device values become superior to the conventional single-gate SOI MOSFET. To

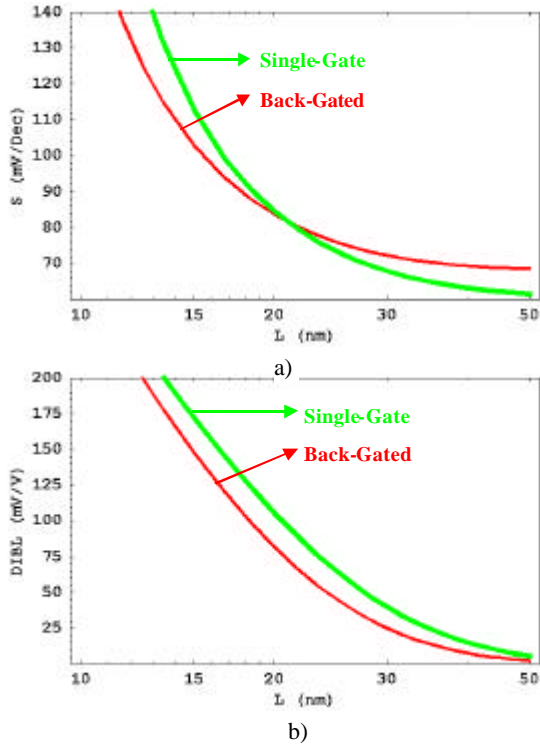


Fig. 2. shows the inverse sub-threshold slope and DIBL values for back-gated and single-gate SOI MOSFET vs. the gate-length. The parameters are projected values for $L_G = 25$ nm technology node: $t_{Si}=10$ nm, $t_{Fox}=0.9$ nm, $t_{Box}(\text{Back-gated})=3$ nm, $t_{Box}(\text{Single-gate})=50$ nm.

illustrate this, the inverse sub-threshold slope and DIBL for back-gated and single-gate devices are plotted vs. gate-length in **Fig. 2** for same device parameters that are projected for 25 nm technology node [8]. It is clear that for small gate lengths, back-gated SOI MOSFET have superior electric characteristics.

2. Experimental and Simulation Results for Scaling

In our experimental work, back-gated SOI MOSFETs are fabricated by bonding a back-gate patterned wafer prior to front-gate and the residual transistor processing [6]. Here, we compare transistor characteristics with back-gate to those of conventional single-gate SOI transistors on the same chip. For control, we employ $0.25 \mu\text{m}$ as the gate-length, and the structures have been

fabricated without any intentional channel doping. This absence of channel doping is intentional in order to clearly articulate, experimentally, the consequences of back-gate control in thin single-crystal silicon device structures. The transfer characteristics of different back-gate biases and the conventional single-gate device are plotted in **Fig. 3**. The effect of back-gate bias on DIBL is shown in **Fig. 4**. Since the constant back-gate potential prevents the source-drain field penetration into the back-channel, the DIBL for back-gate biased devices is much lower (25-50 mV) than the single-gate SOI devices (72 mV) in conformity with the theoretical model. However, the inverse sub-threshold slope for back-gated transistors is higher than the single-gate transistor (**Fig. 4**) due to the capacitive coupling between front and back-gates as projected by the theory for long-channel devices. Drift-diffusion simulation results of back-gated and single-gate SOI MOSFET's for $L_G = 35$ nm are also compared here to look at scalability. For reverse back-gate bias range of interest (the channel is totally depleted), the inverse sub-threshold slope of back-gated device (~ 85 mV/decade) is lower than the one for single-gated counterpart (100 mV/decade) (**Fig. 5**). Together with long-channel results, this confirms the theory that the inverse sub-threshold slope of back-gated device is larger than single-gated device for long-channel, but since it has a smaller natural scale length, back-gated device inverse sub-threshold slope is lower for shorter gate lengths.

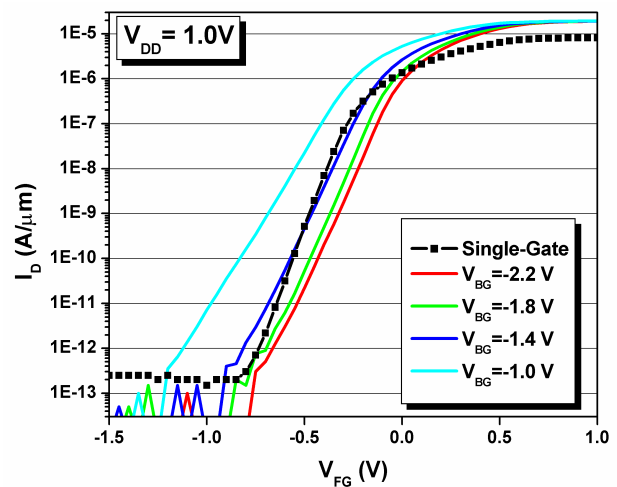


Fig. 3. shows the transfer curve for back-gated and single-gate SOI MOSFET vs. the front-gate bias

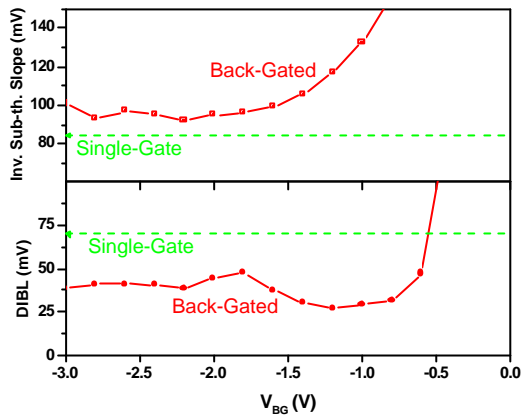


Fig. 4. shows the experimental DIBL and inverse sub-threshold slope measurements for back-gated and single-gate SOI MOSFET structures. The devices are on the same chip with $W/L=1 \mu\text{m}/0.25 \mu\text{m}$.

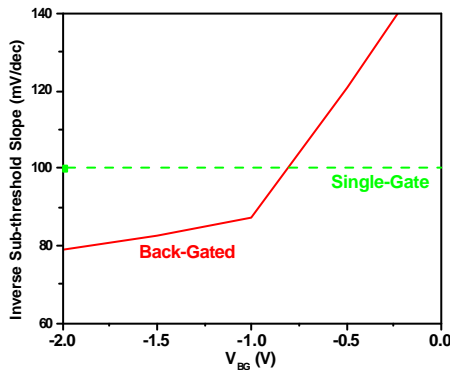


Fig. 5. shows the simulation results of inverse sub-threshold slope for back-gated and single-gate SOI MOSFET structures with $L_G = 35 \text{ nm}$.

3. Understanding the Device by Using Back-Gate

Since the back-gate positioning and sizing is independent from the front-gate, this device also provides a tool to understand the implications of electrostatics as the device dimensions are shrunk. We have employed this to understand the implications of the thinning or thickening of the two-dimensional electron gas at the source-end through electrostatics, and its consequence for the transport as observed in the current-voltage characteristics. This is achievable through bias when the back-gate is towards the source-end. Similarly, when the back-gate is towards the drain-end and the source-end back-gate-free, the source-end injection changes as does the two-dimensional shielding at the drain-end. Thus, the device provides a powerful tool for analysis of the consequences of electrostatics on the transport in the structure.

In the long-channel approximation, non-self-aligned reversed-bias back-gated device can be approximated as two transistors with different threshold voltages in series. The two different possible configurations are back-gate shifted to the source-side (BG-S) and the back-gate shifted to the drain side (BG-D). Since the back-gate is reverse biased, in BG-S configuration the high- V_T transistor is at the source-side (at high back-gate voltage) whereas in BG-D configuration high- V_T transistor is at the drain-side (at high back-gate voltage). Both configurations have the same electrical results for low drain-biases (**Fig. 6**) since the lateral positioning is significant only when lateral electric field is considerable with respect to cross-sectional field. In the sub-threshold region, the current is barrier-modulated and the potential barrier peak of front-interface, which is within the high- V_T transistor, determines the transport constraint. In BG-D configuration, the drain-control over this barrier is more than in BG-S configuration because of the drain proximity to this peak. Therefore, although they show similar characteristics for low drain-bias, for high drain-bias condition, threshold-voltage shift due to DIBL is higher when BG is shifted to the drain-side (BG-D), as supported with experimental results of **Fig. 6**.

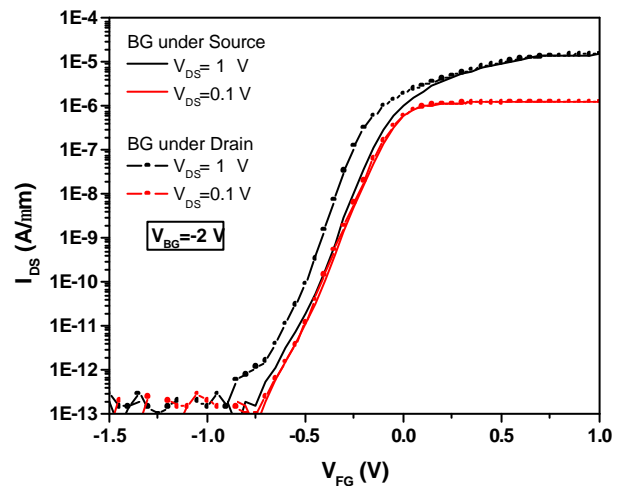


Fig. 6. shows the experimental transfer curves for source-side shifted back-gate (BG-S) and drain-side shifted back-gate (BG-D) for low and high drain biases with $L_G = 250 \text{ nm}$.

Output characteristics for both configurations (back-gate shifted to source and back-gate shifted to drain) are plotted in **Fig. 7**. In the linear (triode) region, because of the low-drain bias, the outputs are similar due to a balancing of two-dimensional effects in total charge at

source side. Beyond saturation, BG-S follows a conventional long-channel device behavior and stays almost constant due to the buffering from the low- V_T device that exists between the high- V_T device and the drain. However, since in BG-D configuration, the high- V_T transistor is next to the drain, as the saturation point moves from drain-junction to source with higher drain biases, the channel length of the high- V_T device is reduced [9]. Thus, the channel-length modulation beyond-saturation causes the drain-current of BG-D configuration to increase with $1/(L \cdot L)$.

High-drain bias transfer curves for different back-gate biases are plotted for both BG-S and BG-D configurations in Fig. 8. As stated earlier, for negative biased back-gate, BG-D configuration has lower threshold-voltage due to DIBL. The amount of threshold voltage shift achievable through the back-gate is also larger when the back-gate has stronger source-end control. For ground or positive biases, the back-channel has a lower potential than the front-channel at negative front-gate voltages and the positioning of high- V_T transistors are switched. The plateauing at negative front-gate voltages in these characteristics arises from the conduction through the bulk of the thin silicon. Thus, the threshold-voltage lowering and increase in drain-current is expected for BG-S configuration for this region of operation. Note that at negative voltages on gate, whether on the front or on the back, there is band-edge movement that provides for conduction since the two gates pull the bands either towards the conduction or towards the valence bands.

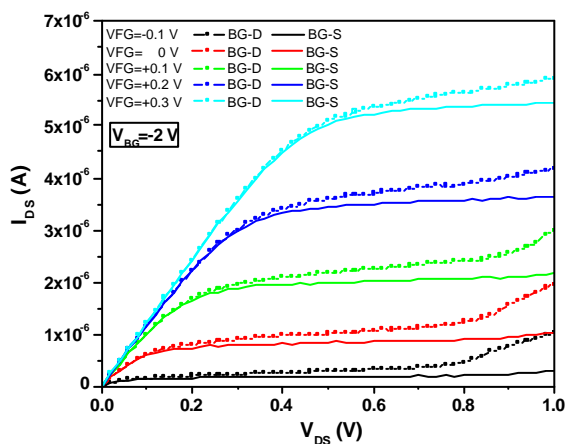


Fig. 7. Experimental output characteristics for both source-side shifted back-gate (BG-S) and drain-side shifted back-gate (BG-D) configurations are plotted for $L_G = 250$ nm.

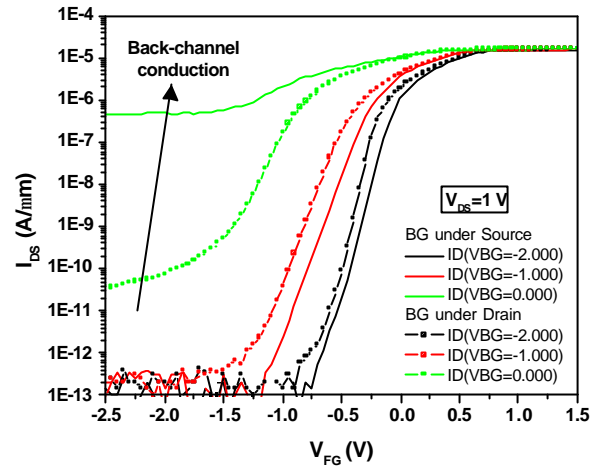


Fig. 8. shows the experimental transfer curves for source-side shifted back-gate (BG-S) and drain-side shifted back-gate (BG-D) for different back-gate biases with high- V_{DS} for $L_G = 250$ nm.

III. BACK-FLOATING GATE NVRAM

1. Back-Floating vs. Front-Floating Gate

Conventional floating-gate non-volatile memory structures (Fig. 2d), where stored electrons screen the channel from the control gate, are limited in dimensional scaling for power and speed by: 1) limitations to gate-stack insulator thickness to ensure charge retention; 2) inefficiencies of hot-electron injection processes as dimensions approach many 10^2 's of nanometers; 3) poor electrostatic control due to nonscaling of insulators; and 4) constraints placed on cell size by processes for isolation and floating gate definition. By providing the floating gate on the back of the thin silicon-on-insulator (SOI) channel, this problem can be addressed (Fig. 2c) while keeping the transistor geometry the same. Since the two gates are separate, the floating back-gate can be oversized to increase the overlap in the drain extensions and hence provides efficient injection for NOR-type nonvolatile memory cell. Simultaneously, good electrostatic control of the transistor through scaling of read-gate oxide, etc., occurs and hence good low voltage operation is achieved for read process as well as for charge transport during writing. The difference between the use of charge screening through the floating gate in the two approaches (front and back) is that the front-floating gate charge screens the induced mobile charge in the channel, while the back-floating gate charge

affects the field and the barrier on the back of the channel and thus influences the net effective depletion charge.

Charge from the channel screens the high programming biases of the back-gate/substrate, which helps maintain reliability of the top read oxide, but the reliability of the back-oxide is affected by similar constraints as that of the front-floating gate structures although it is subject to smaller process-induced damage. The endurance and retention are a function of the quality and thickness of the oxide as well as process-induced effects. Since non-volatility requires a minimum oxide thickness to prevent charge leakage, the fundamental constraints for endurance and retention in this structure are not likely to be any different from that of the front-floating gate structures. Since the read operation is decoupled from storage function, the device structure is also more immune to read-disturb and maintain large improvements in sub-threshold slope in the programmed state.

2. Hot Electron Monte Carlo Simulations

Modeling of hot-carrier injection process involves a self-consistent solution of the Poisson/Monte Carlo simulation of BTE using DAMOCLES [10] and the hot carrier tunneling calculation is performed using the obtained velocity, energy, and carrier distribution coupled to the transmission coefficients obtained using WKB approximation [11]. The energy-loss length scale coupled to the velocity overshoot and transmission coefficient has a significant impact to the net flux of electrons available for injection into the floating gate.

The coupling of these two considerations leads to the importance of overlap between the floating gate and the off-equilibrium channel region for efficient injection. Importance of this overlap (referenced to the read/sense gate edge) of the floating gate for efficient coupling of hot electrons is illustrated by the hot-carrier distribution near the drain junction (for a 20 nm overlap) and total injection current density for different overlap lengths in **Fig. 9**. As apparent, an overlap of 20-25 nm allows for coupling of >90% of the hot carriers in the channel and the maximum injection density occurs at 15 nm in the drain junction, consistent with the energy relaxation length scale. Such an overlap cannot be provided by

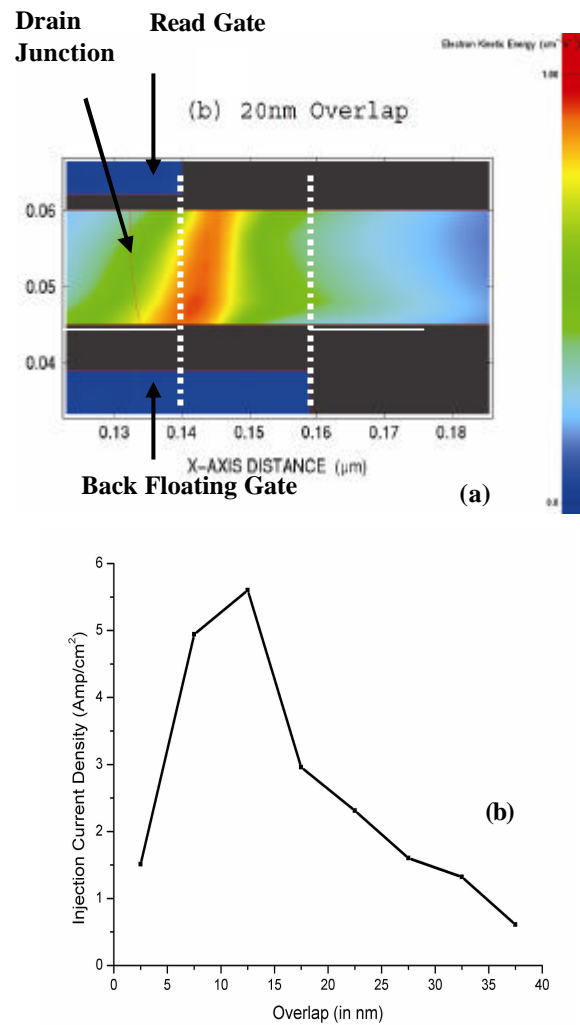


Fig. 9. (a) Energy kinetic energy distribution near the drain during programming of a back floating gate for 20 nm overlap (b) Total injection current density into the floating gate as a function of increasing overlap dimension showing efficient coupling.

front-floating gate structures, but can be by back-floating gate structures. **Fig.10** shows the threshold shift as a function of time for both back-floating gate (with 20 nm overlap) and conventional flash cell using the same injection/control oxide design rules and bias and comparing it to a more relaxed gate stack. Charging times of order of μs are required for a threshold voltage change of $\sim 1\text{V}$ for back-floating gate cell whereas the conventional Flash, due to poor injection efficiency, has charging times which are one or two orders of magnitude slower.

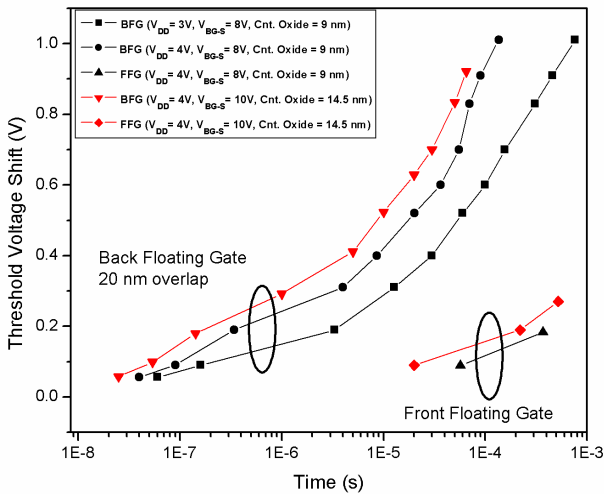


Fig. 10. Simulated programming characteristics of the back-floating gate and conventional front-floating gate memory for different bias conditions and cell designs. The black curves are for cell design with control oxide of 9 nm. The red curve is for a more relaxed control oxide (14.5 nm) design with higher control gate bias (10 V).

3. Measurement Results for NVRAM

We fabricate the back-floating NVRAM using the same technique. The differences essentially lie in the layouts and whether back-gates are connected or not. Thus, even the back-gated transistors provide a means for analyzing the back-gated NVRAM characteristics. The transfer characteristics for a 0.25 μm gate-length device are shown together with its transistor operation in **Fig. 11**. Since the channel is nominally undoped, when the electrons are erased from the back-floating gate, there is a weak inversion at the bottom interface due to the work-function difference. Thus, the current ratio for the read operation between the charged and erased states can be as large as seven orders of magnitude at negative gate biases. **Fig. 12** shows transfer curves for different back-gate biases for contacted back-gate and when the back-gate probe is lifted for that voltage level. Due to the larger capacitance associated with probe pads, the potential does not change upon the lifting of the probe. This allows a clear measurement, without injection-caused degradation, of the consequences to the device transport for different potentials that arise from different charge stored in the back-gate (floating). The characteristics of **Fig. 12**, therefore show the memory window that can be achieved in these structures by storage of charge on the back-gate.

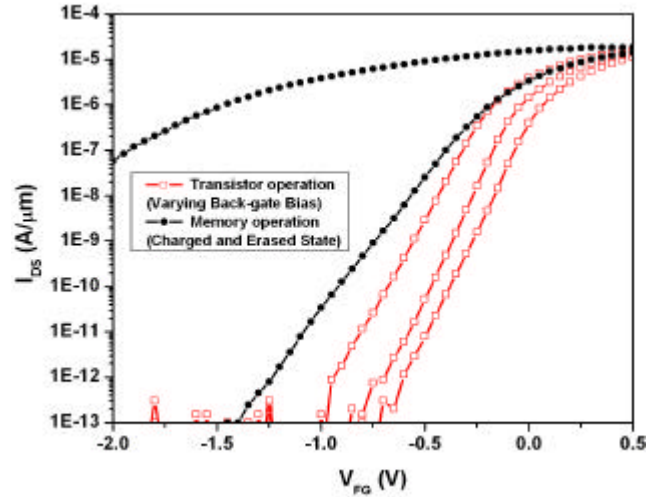


Fig. 11. shows the experimental results for back-floating gate memory operation. The erased and charged state transfer curves are plotted together with back-gate biased transistor transfer curves for $V_{BG} = -3 \text{ V}, -1.8 \text{ V}, -1.2 \text{ V}$ ($L_G=250 \text{ nm}$).

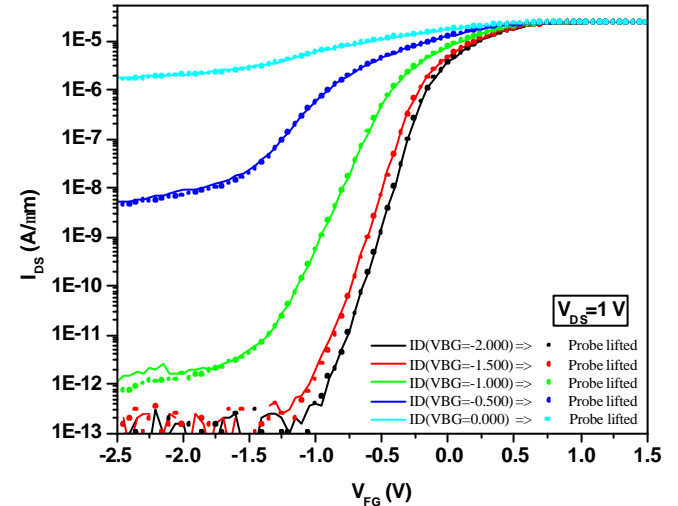


Fig. 12. shows transfer curves for different back-gate biases for contacted back-gate and when the back-gate probe is lifted for that voltage level ($L_G = 250 \text{ nm}$).

IV. CONCLUSION

The short-channel characteristics of back-gated SOI MOSFET are analyzed using the two-dimensional Poisson's equation. The obtained natural length scale of back-gated SOI MOSFET is always smaller than of the single-gate SOI MOSFET. Accordingly, the inverse subthreshold slope and DIBL are found to scale better for the back-gated transistor. This is supported by experimental and simulation results. The back-gate structure provides a convenient means to understanding

the transport effects and connecting them to electrostatics – for both the transistor-mode and the memory-mode of operation. These results have clarified the role of source-side injection and the consequences of electrostatics on the transport. Back-floating gate NVRAM is simulated for hot-electron injection and is demonstrated to be both more scalable and time-efficient compared to the conventional floating-gate memory. The experimental realization of this memory is also shown. The ability to control threshold-voltage for power, the ability to achieve high density because of the low areal penalty of the underlying gate in the buried structure, and the ability to make non-volatile memories in a simple technology make this approach a powerful method for addressing nano-scale electronics issues.

using Back-Floating Gates,” in *IEEE Trans. on Nanotechnology*, vol.1, p. 247, 2002.

Biography of the authors are not available at the time of publication

REFERENCES

- [1] H.-S.P. Wong, D.J. Frank, P.M. Solomon: “Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET’s at the 25 nm channel length generation,” in *IEDM Tech. Dig.*, pp. 407, 1998.
- [2] T. Tanaka, H. Horie, S. Ando, S. Hijiya: “Analysis of p+ double-gate thin-film SOI MOSFET’s,” in *IEDM Tech. Dig.*, pp. 683, 1991.
- [3] R.H. Yan, A. Ourmazd, K.F. Lee: “Scaling the Si MOSFET: from bulk to SOI to bulk,” in *Transactions on Electron Devices*, vol. 39, pp. 1704, 1992.
- [4] T. Ernst, S. Cristoloveanu: “Buried oxide fringing capacitance: A new physical model and its implication on SOI device scaling and architecture,” in *IEEE Int. SOI Conference*, pp.38, 1999.
- [5] Y. Tosaka, K. Suzuki, T. Sugii: “Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET’s,” in *Electron Device Letters*, vol. 15, pp.466, 1994.
- [6] U. Avci, S. Tiwari: “Back-gated MOSFETs with controlled silicon thickness for adaptive threshold-voltage control,” in *Electronics Letters*, vol. 40, pp. 74, 2004.
- [7] K.K. Young: “Short-channel effect in fully depleted SOI MOSFETs,” in *Transactions on Electron Devices*, vol. 36, pp.399, 1989.
- [8] International Technology Roadmap for Semiconductors, 2003, <http://public.itrs.net/>.
- [9] Y. Taur, and T. H. Ning: “Fundamentals of modern VLSI devices,” Cambridge University Press, 1998.
- [10] S. E. Laux, M. V. Fischetti, and D. J. Frank: “Monte Carlo analysis of semiconductor devices: The DAMOCLES program,” in *IBM J. Res. Develop.*, vol.34, p. 466, 1990.
- [11] A. Kumar and S. Tiwari: “Scaling of Flash NVRAMs to 10’s of nm by Decoupling of Storage from Read/Sense