

Editorial

We are very pleased to announce the special issue on “Scaled Nano Devices”. As semiconductor device technology progresses towards the sub-10 nm regime, the issues of design, technology, and modeling of scaled silicon devices becomes more challenging and important. JSTS, one of the emerging semiconductor journals dealing with both technology and science, was planning to have a special issue on scaled nano devices, and we selected seven excellent papers in this issue.

The first two papers dealt with the new MOS devices with double gates, which are called FinFETs. The first paper is a review paper on the technology of FinFETs. The second paper is on the design and modeling of body-tied FinFETs. The third paper is on SOI MOSFETs and NVRAMs related to the SOI MOSFETs. The fourth paper presented the modeling results of gate tunneling current in scaled nano devices. The fifth paper is on the simulation technique for the quantum effects in nano devices. The next two papers are on the process technique of silicon nano devices. The sixth paper is on the nanolithography for silicon nano devices. Finally the last paper is on one of the most important processing techniques in the fabrication of nano devices : CVD.

We would like to express sincerely thanks to all authors for paper submission and sharing research progress with us.

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Guest editor of this special issue