

Editorial

We are very pleased to announce the special issue on ;Device Reliability;. As semiconductor device technology progresses towards the sub-nm regime, the issues of design, processing, testing and reliability evaluation becomes more challenging and critical. JSTS, one of the emerging semiconductor journals dealing with both technology and science, was planning to have a special issue, and we selected eight excellent papers in this issue.

The first paper dealt with the process and structural effects on the microelectronics reliability and its failure mechanism. Next two papers regarded semiconductor interconnections, the one for Cu/low-k interconnection and the other for flip chip interconnection. The fourth paper showed the data retention characteristics on FRAM. The fifth paper addressed the edge direct tunneling(EDT) current across thin gate oxide, which affected the circuit performance of analog CMOS. The next two papers are on the device reliability, specially one for silicon MOSFET, and the other for HEMT. Finally the last paper gave us the total study of the electrostatic discharge(ESD) in CMOS, SOI and SiGe.

We would like to express sincerely thanks to all authors for paper submission and sharing research progress with us.

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