

Editorial

The papers of this special issue on SoC(system on a chip) design were selected from the papers published at the two conferences, the IDEC Conference and the SoC Design Conference. The IDEC conference was held on August 28th of 2003 in Daejun, which was organized by IDEC(IC Design Education Center). The SoC Design Conference was held on November 5th and 6th of 2003 in Seoul with the theme of “solutions for mobility and connectivity”, which was organized by IEEK(Institute of Electronics Engineers of Korea). Four papers were selected from the IDEC Conference, and the other four papers were selected from the SoC Design Conference.

The paper “A design of 16-bit adiabatic Microprocessor core” described a 16-bit low-power processor based on ECRL(efficient charge recovery logic), and showed that the power consumption is reduced by a factor of 2.9~3.1 by employing simplified four-phase clock generation and energy recycling operation. The paper “Reconfigurable Hardware Structures for Spreading and Scrambling Operations” proposed area-efficient reconfigurable structures for multi-mode CDMA systems. The paper “3- Transistor Cell OTP ROM Array Using Standard CMOS Gate-Oxide Antifuse” proposed and characterized a new OTP cell structure compatible with standard CMOS technology. The paper “A 3 V 12b 100 MS/s CMOS D/A Converter for High-Speed Communication Systems” showed that the low-glitch switch driving circuits employed to improve linearity and dynamic performance led to spurious-free dynamic range (SFDR) of 64 dB at 100 MS/s with a 10 MHz input sine wave, and the measured DNL and INL were within 0.75 LSB and 1.73 LSB at 12b, respectively.

The paper “Content Switching Network Processor and Scalable Switch Fabric for Gigabit Ethernet” demonstrated that the network processor especially optimized for content switching was developed by integrating components on a single chip by using a 0.18um CMOS process, and that the application of the developed chip to real giga-bit Ethernet environments gave the wire-speed capability. The paper "An Adaptive Spatial Depth Filter for 3D Rendering IP" showed that the memory bandwidth was saved up to 67% by adding a simple hardware filter in a 3D rendering engine. The paper "An 128-phase PLL using interpolation technique" demonstrated that an effective 16GHz clocking was feasible by applying the 128-phase interpolation and design techniques on a 125Mhz clock with a 0.25um CMOS process. The paper "A 622Mbps burst mode CDR with jitter reduction capability" demonstrates a low-jitter burst mode clock and data recovery circuit using a 0.25um CMOS process.

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